

FIG. 1

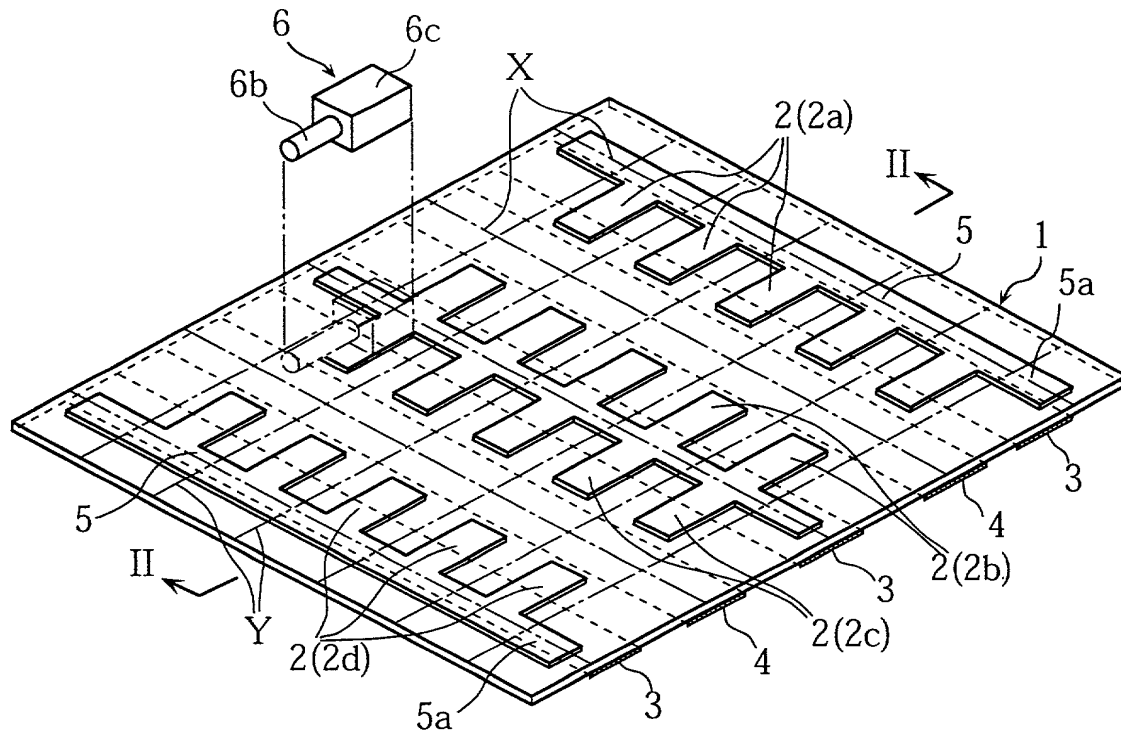
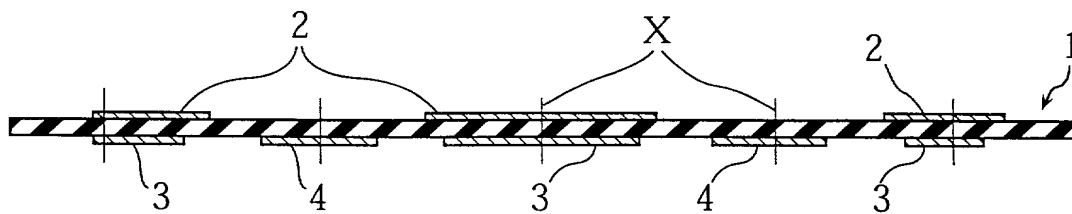


FIG. 2



2/73

FIG. 3

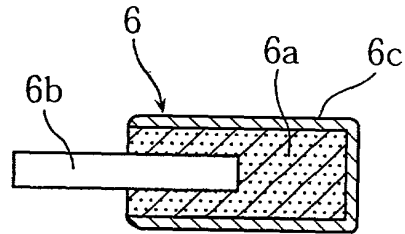
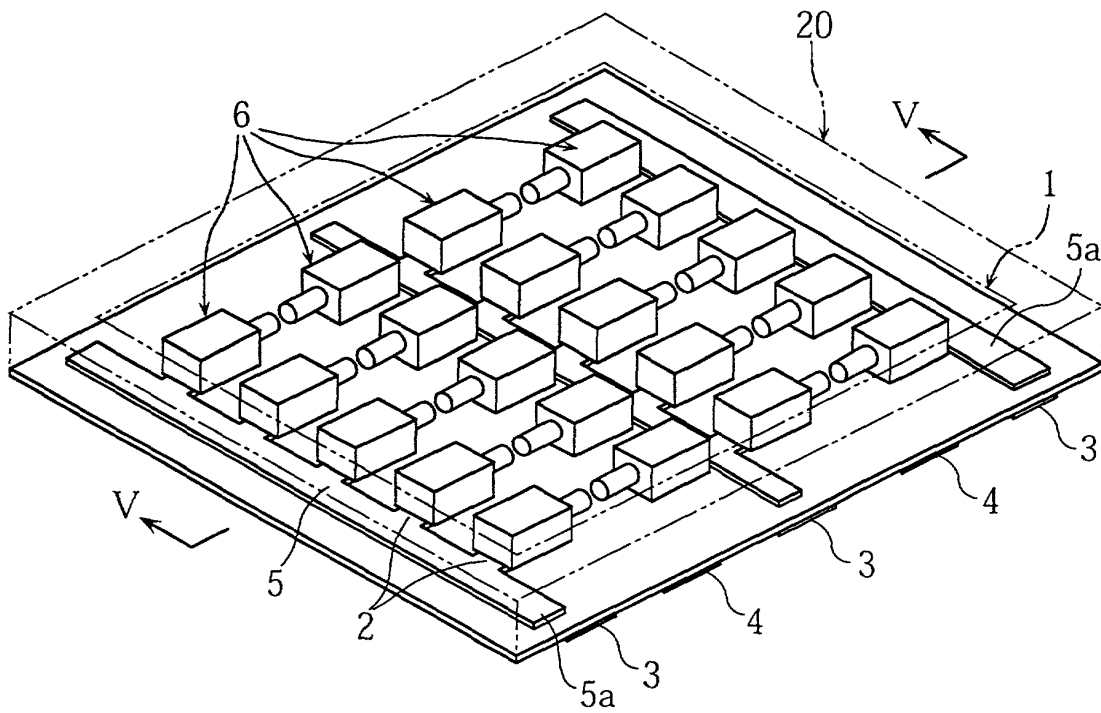
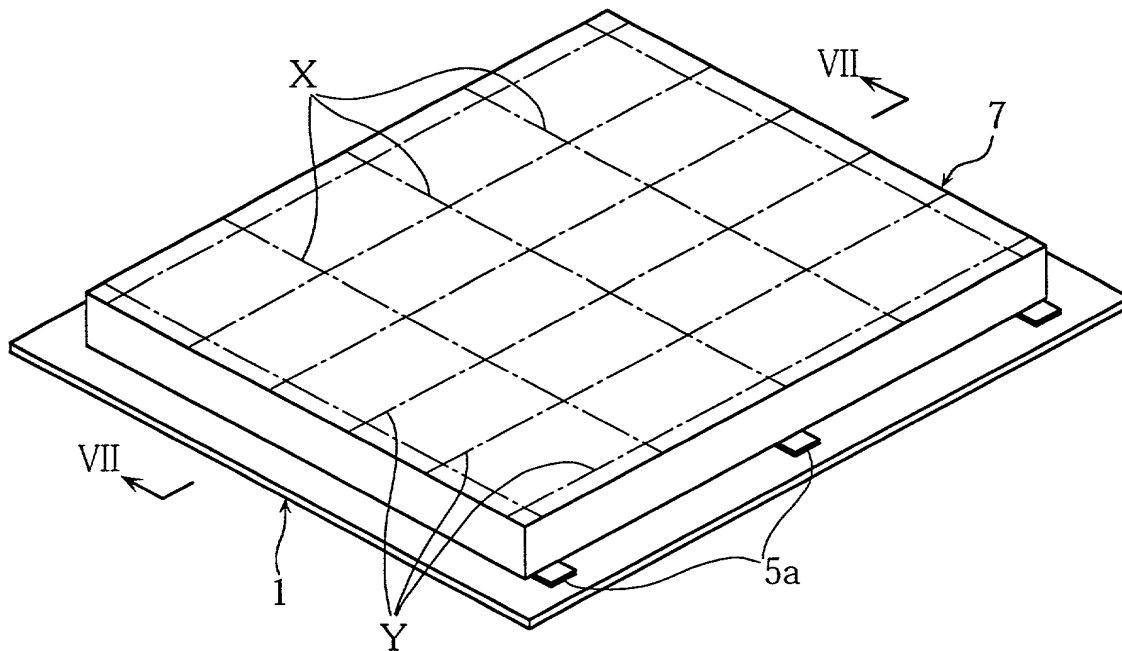


FIG. 4





4/73

FIG. 7

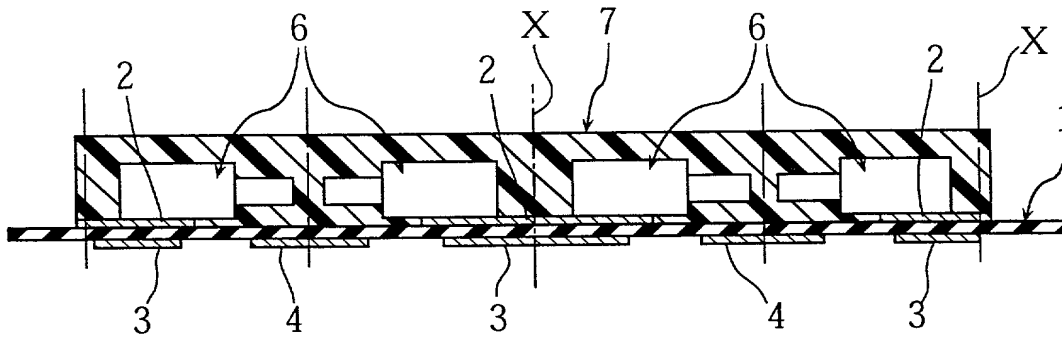
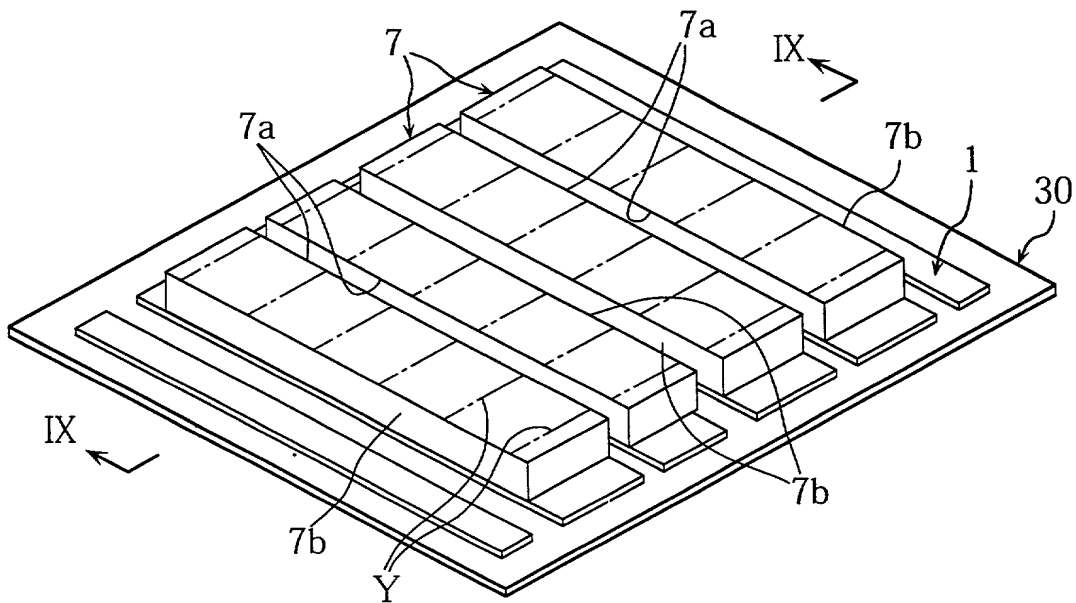


FIG. 8



1008934.10901

5/73

FIG. 9

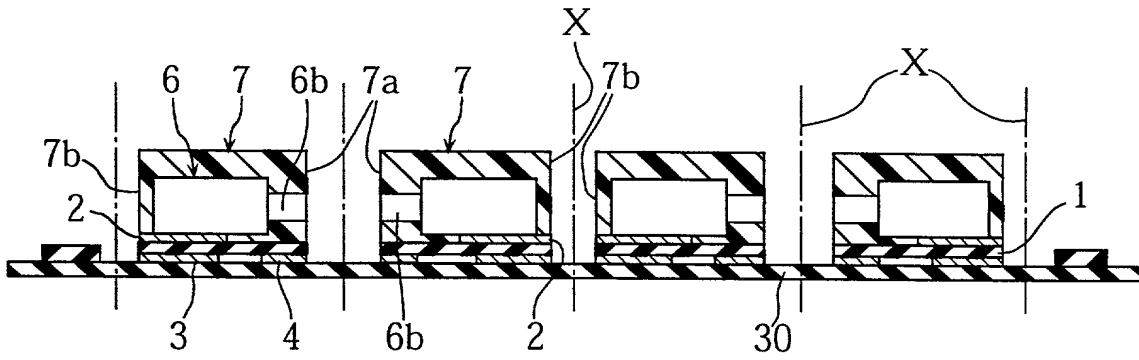
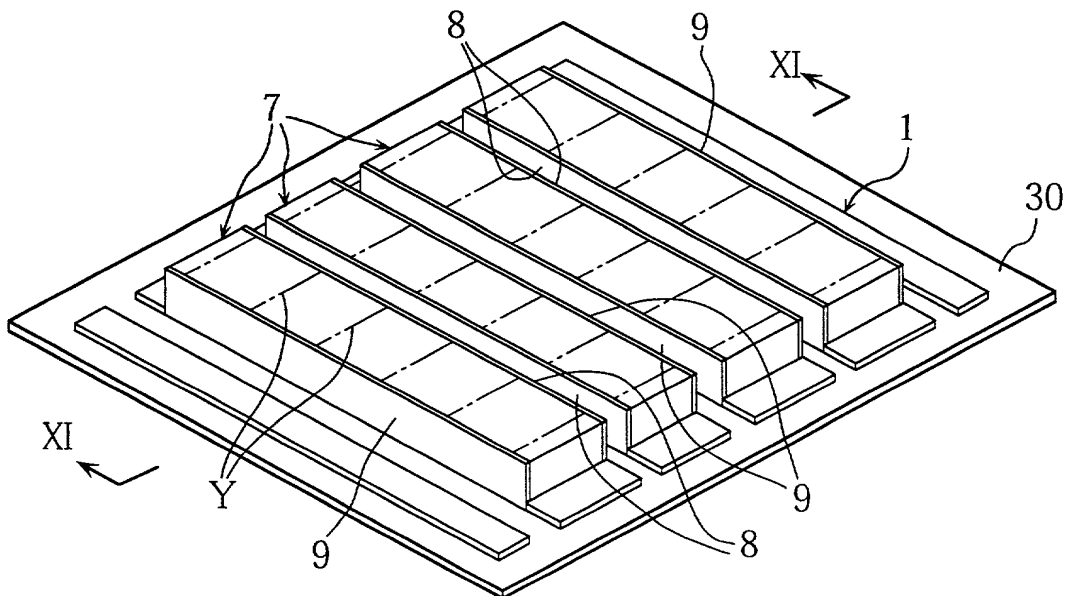


FIG. 10



6/73

FIG. 11

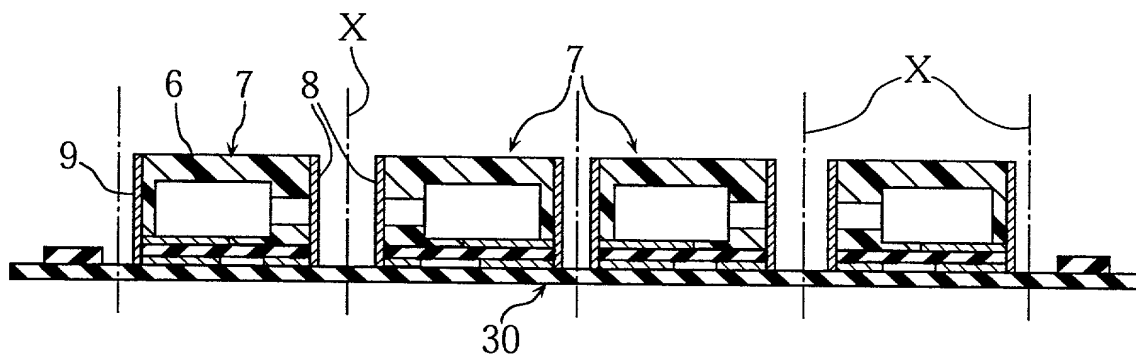
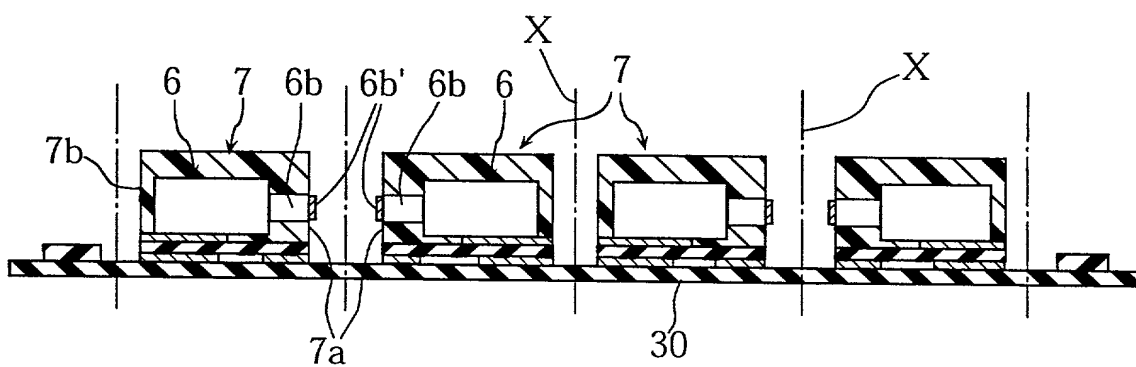


FIG. 12



7/73

FIG. 13

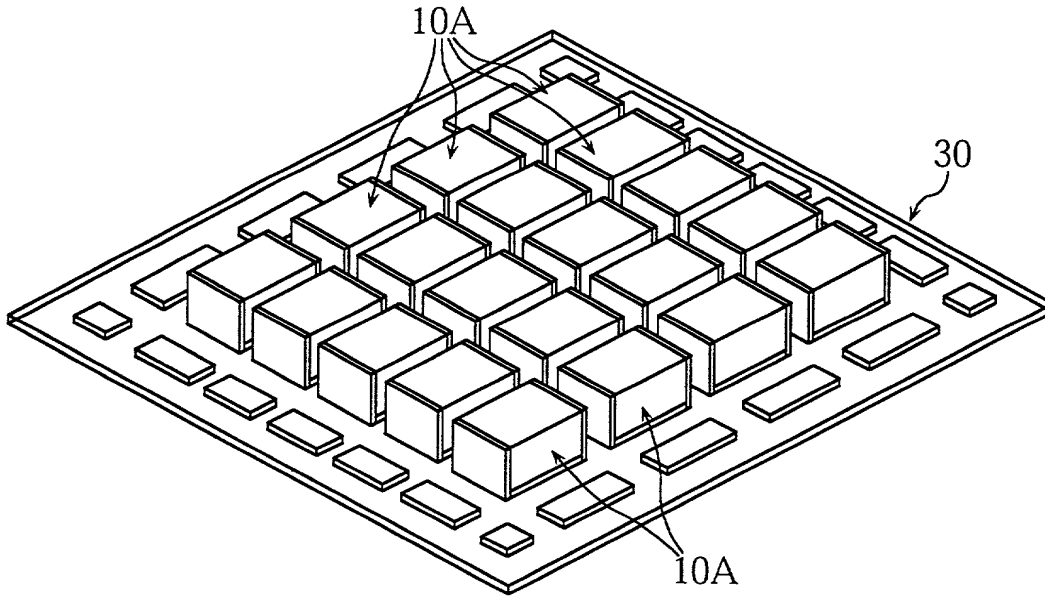
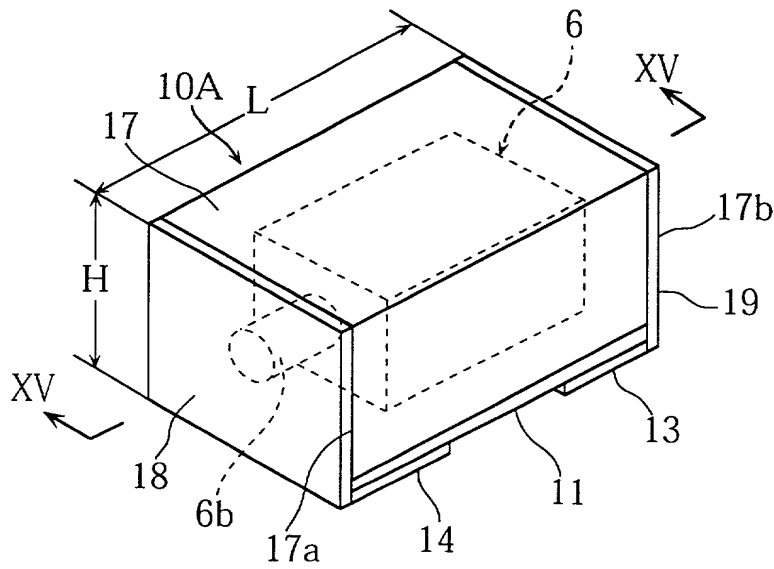


FIG. 14



8/73

FIG. 15

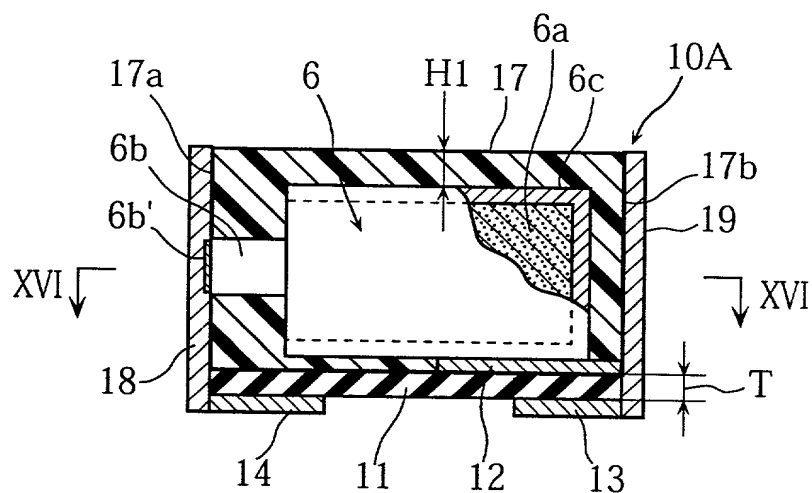


FIG. 16

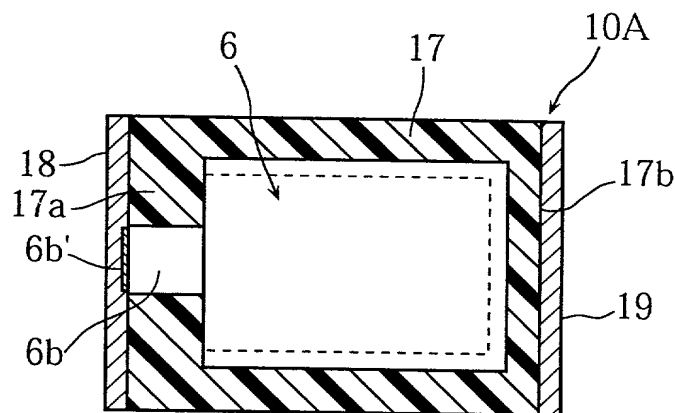
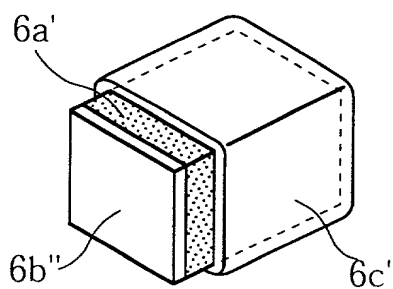


FIG. 17





9/73

FIG. 18

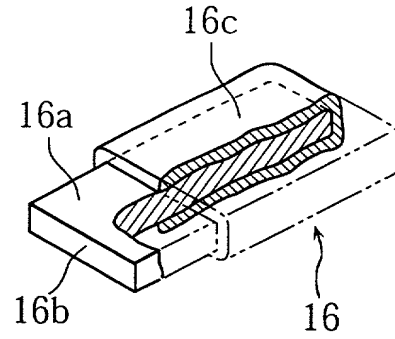


FIG. 19

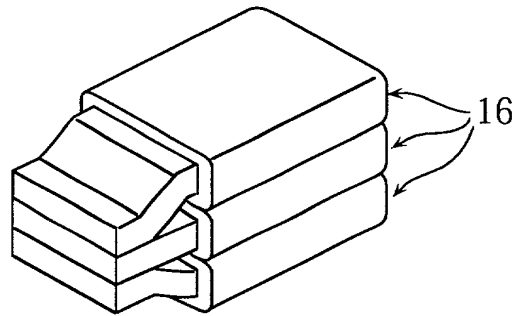


FIG. 20

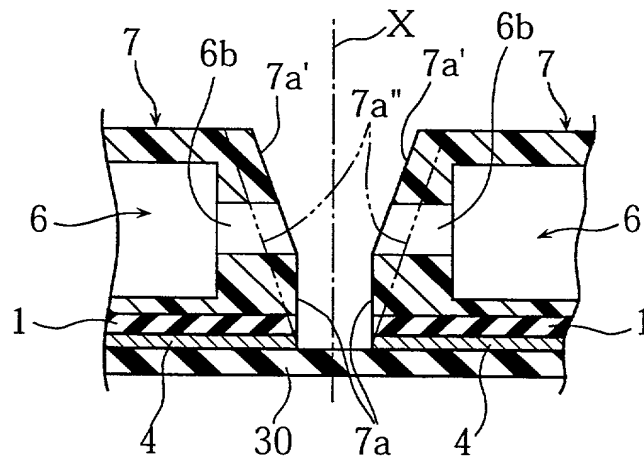
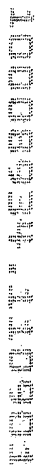
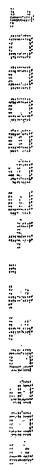


Fig. 10A' is a cross-sectional view of a semiconductor device. It shows a substrate 11 with a central rectangular region 6 defined by a dashed line. This region is surrounded by a layer 12. Above the substrate, there is a layer 17. On the left side, a structure 18 is shown, which includes a layer 17a' and a layer 17a''. A layer 6b is also indicated. The device is shown with a top surface 10A' and a bottom surface 13. A layer 14 is located at the bottom of the central region 6. A layer 19 is located on the right side of the device.

[illegible][illegible]

12/73

FIG. 25

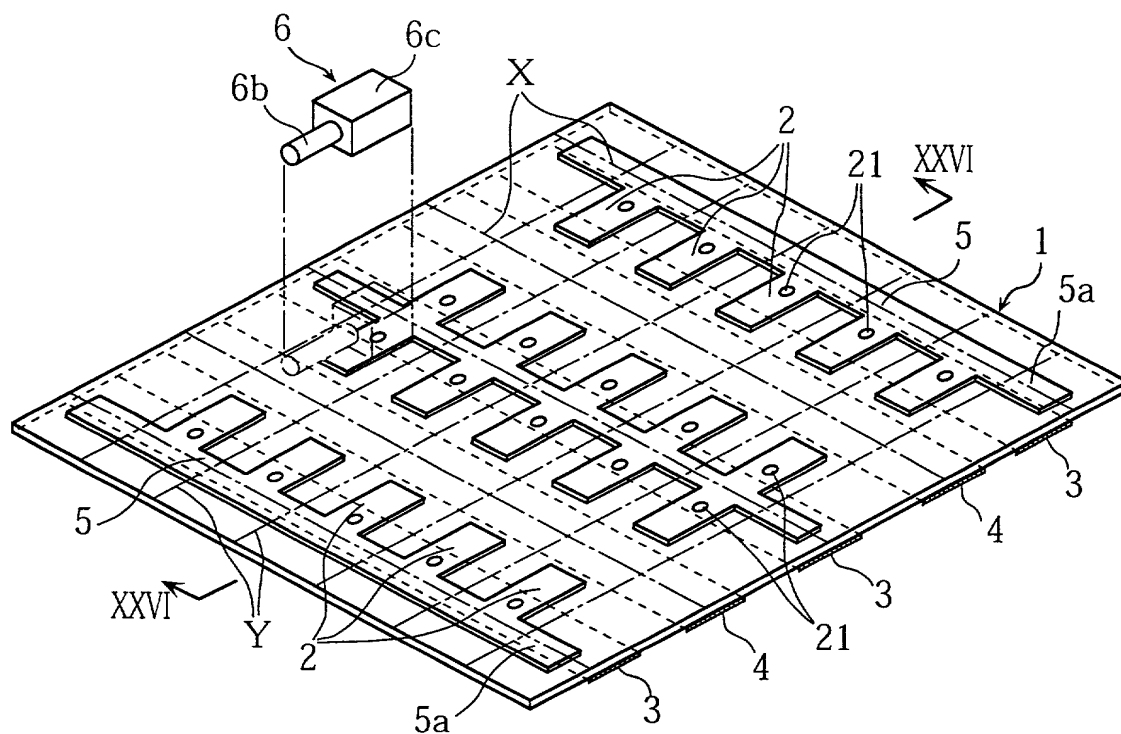
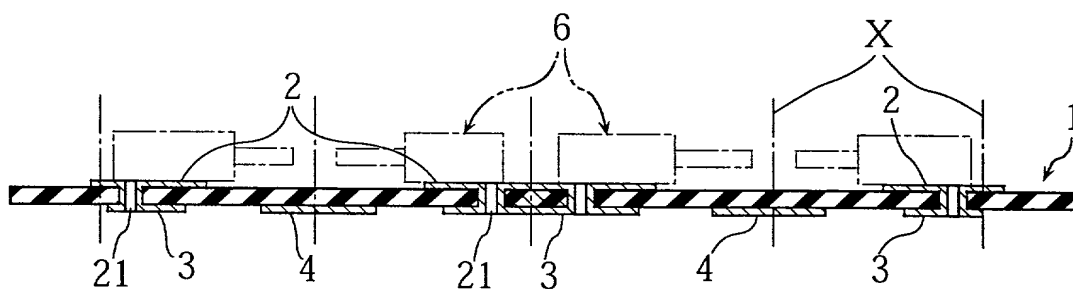


FIG. 26



13/73

FIG. 27

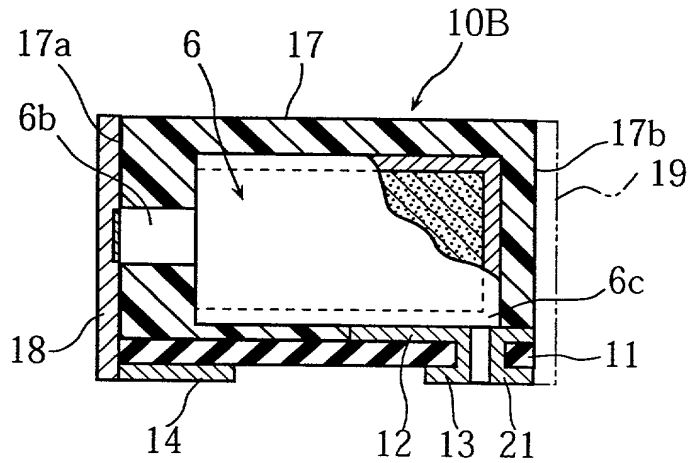
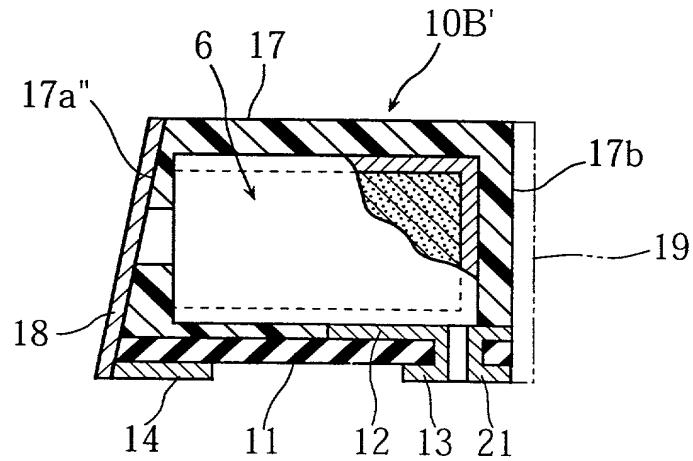


FIG. 28



14/73

FIG. 29

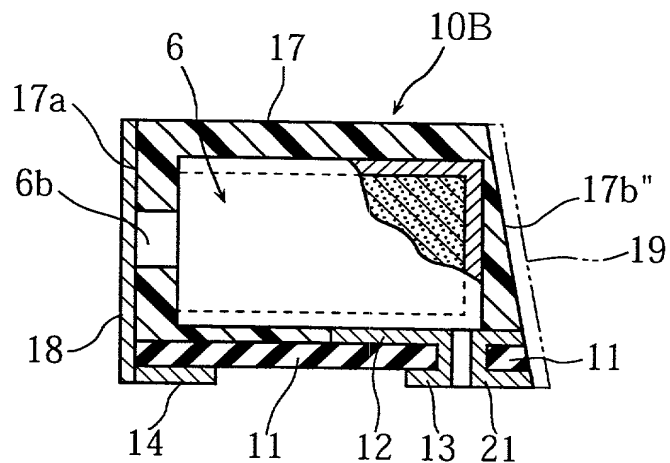
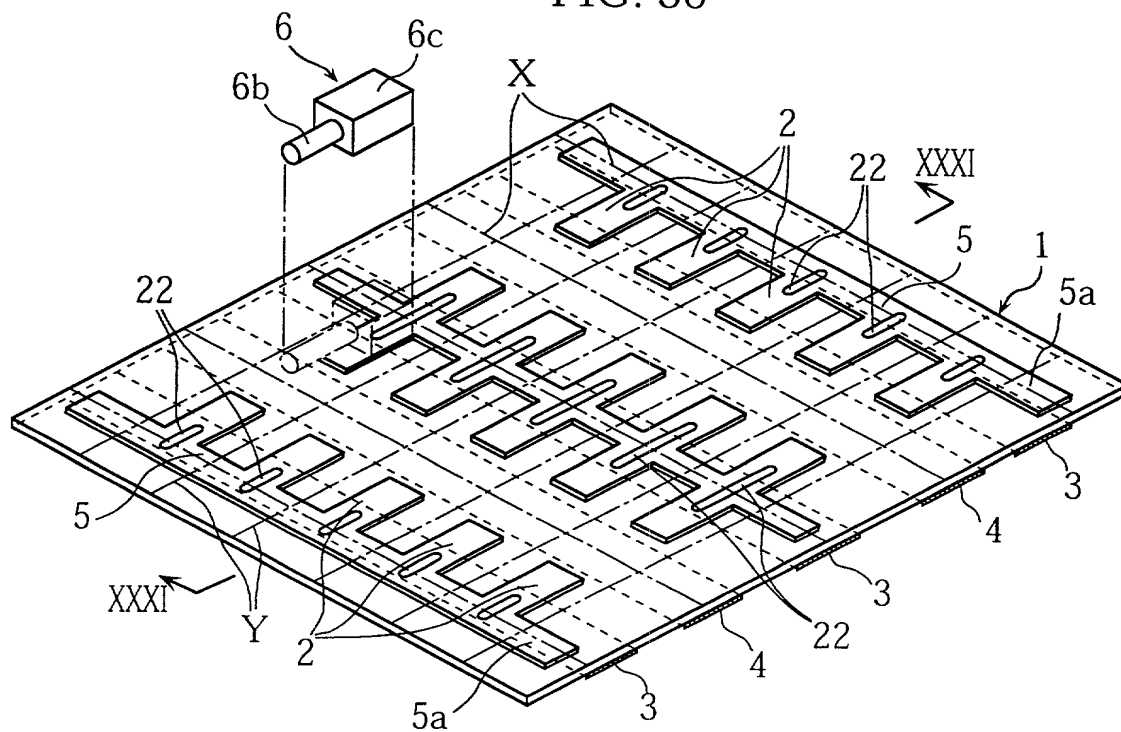
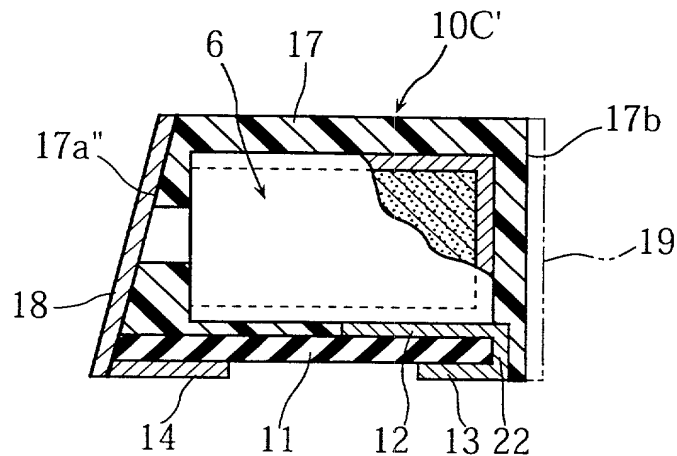


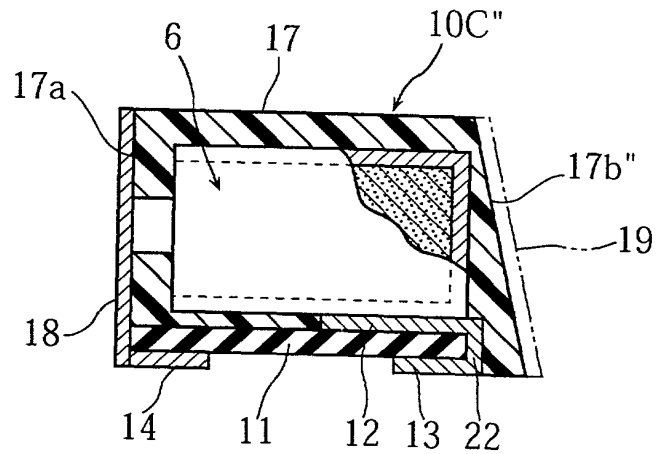
FIG. 30





16/73

FIG. 34





17/73

FIG. 35A

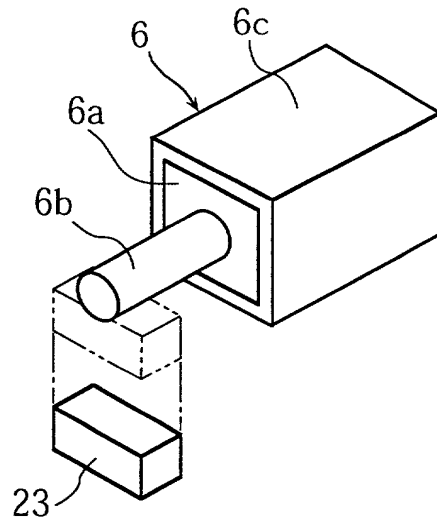


FIG. 35B

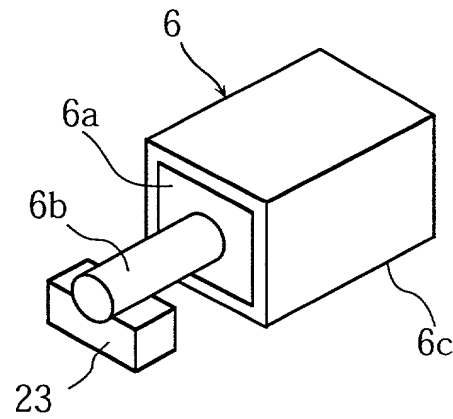
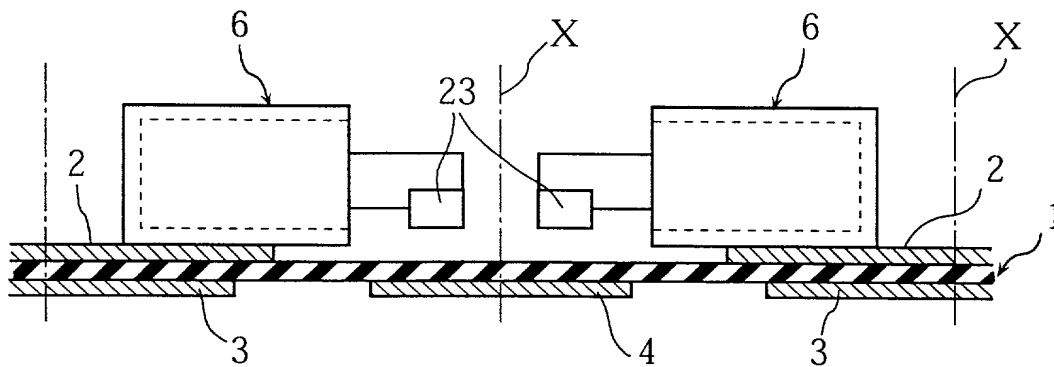


FIG. 36



18/73

FIG. 37

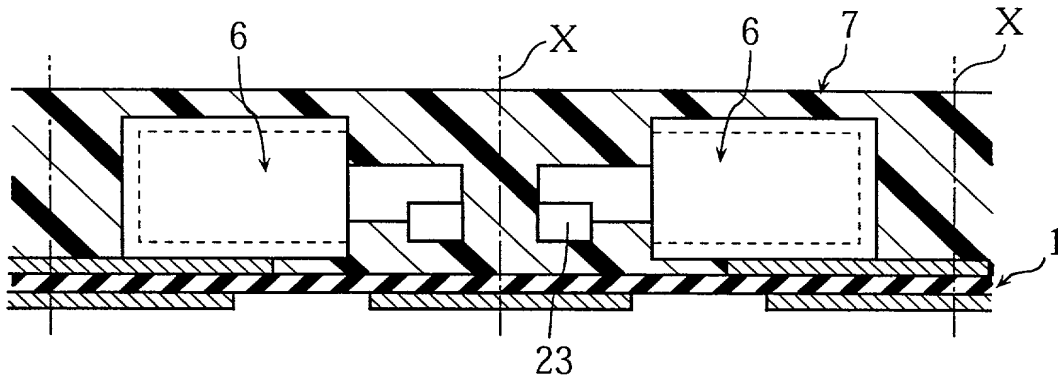


FIG. 38

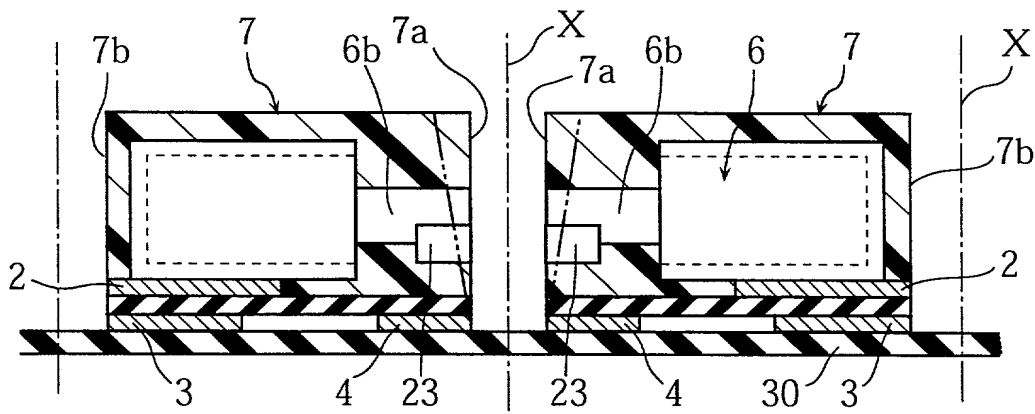
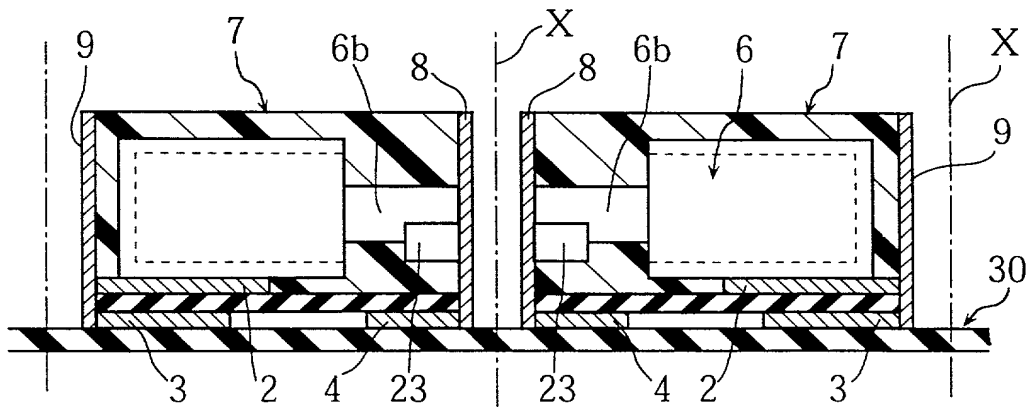


FIG. 39



19/73

FIG. 40

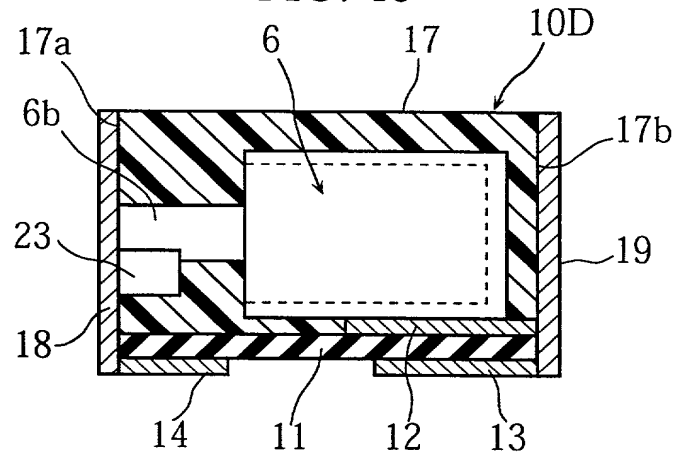


FIG. 41

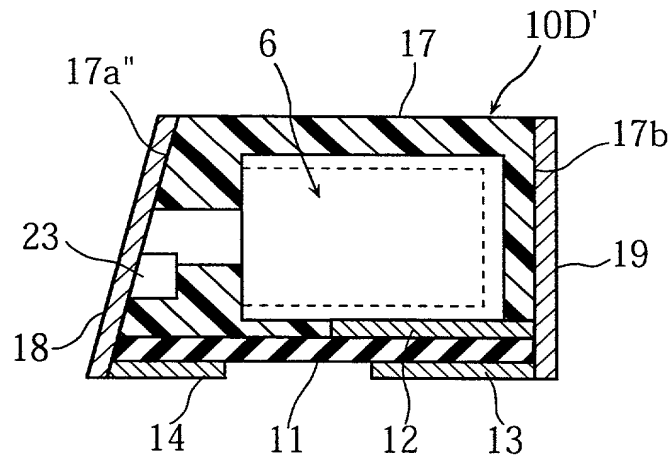
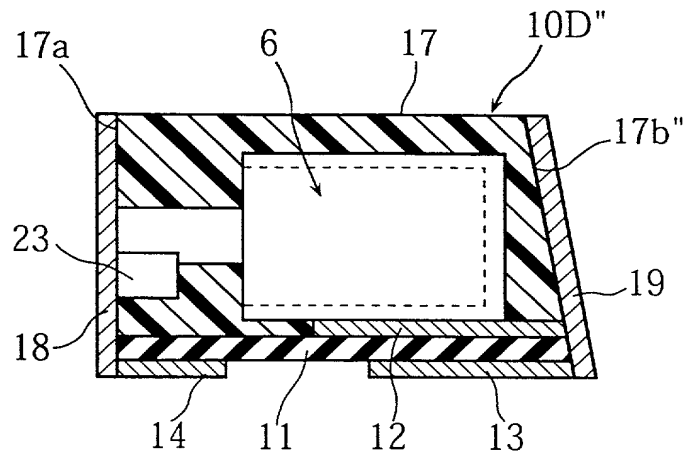


FIG. 42



20/73

FIG. 43

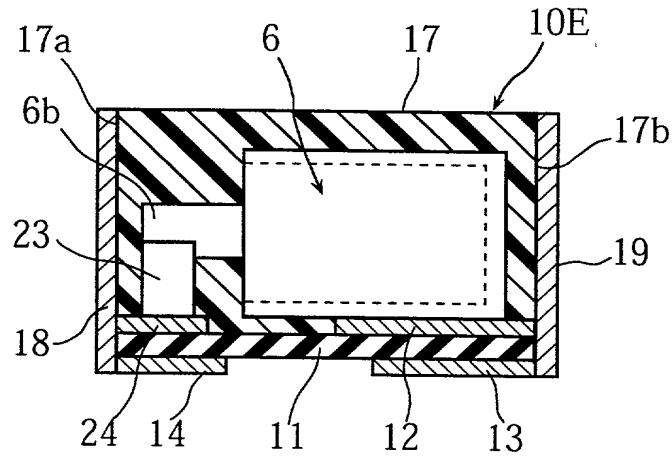
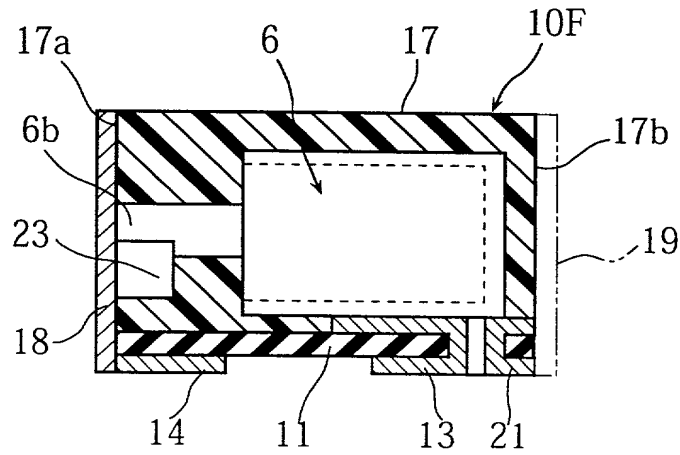


FIG. 44



21/73

FIG. 45

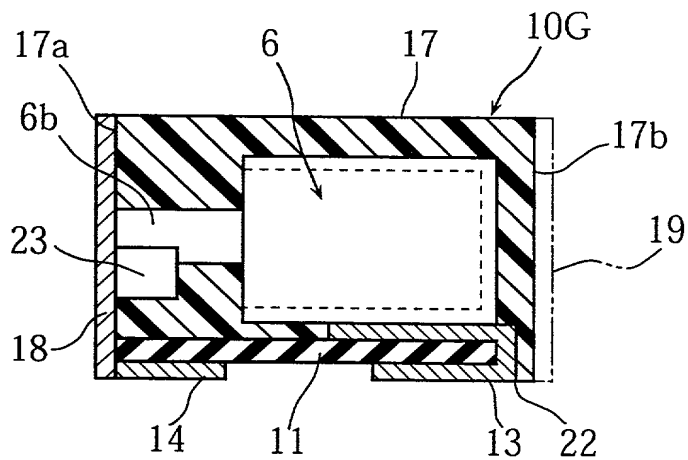
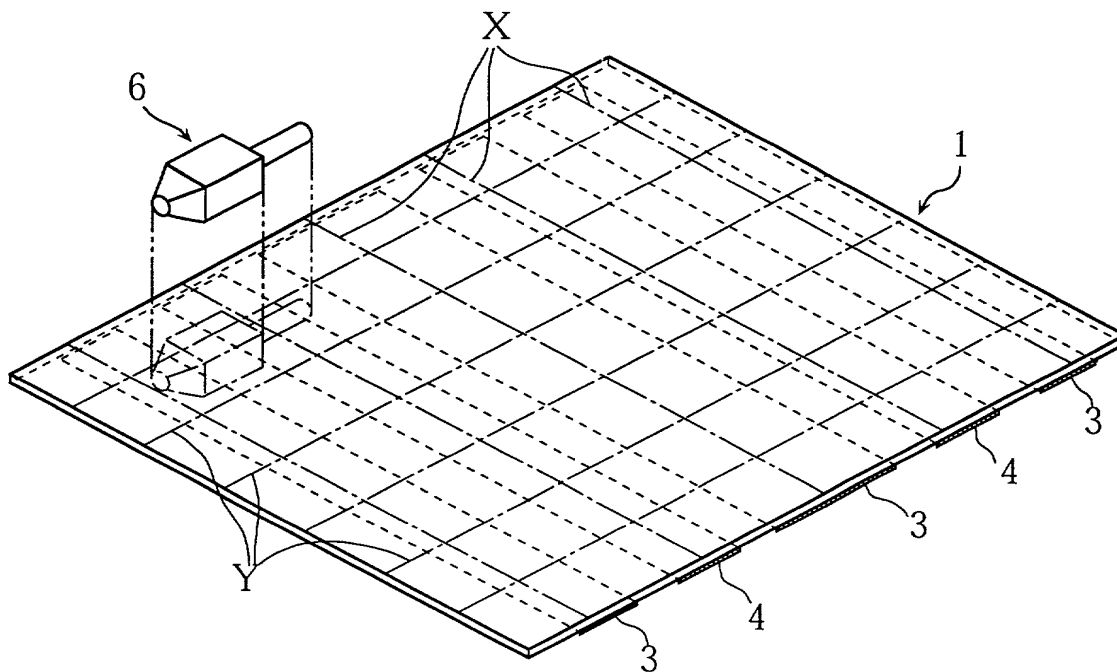


FIG. 46



22/73

FIG. 47

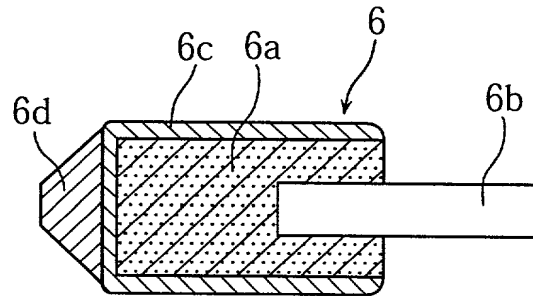
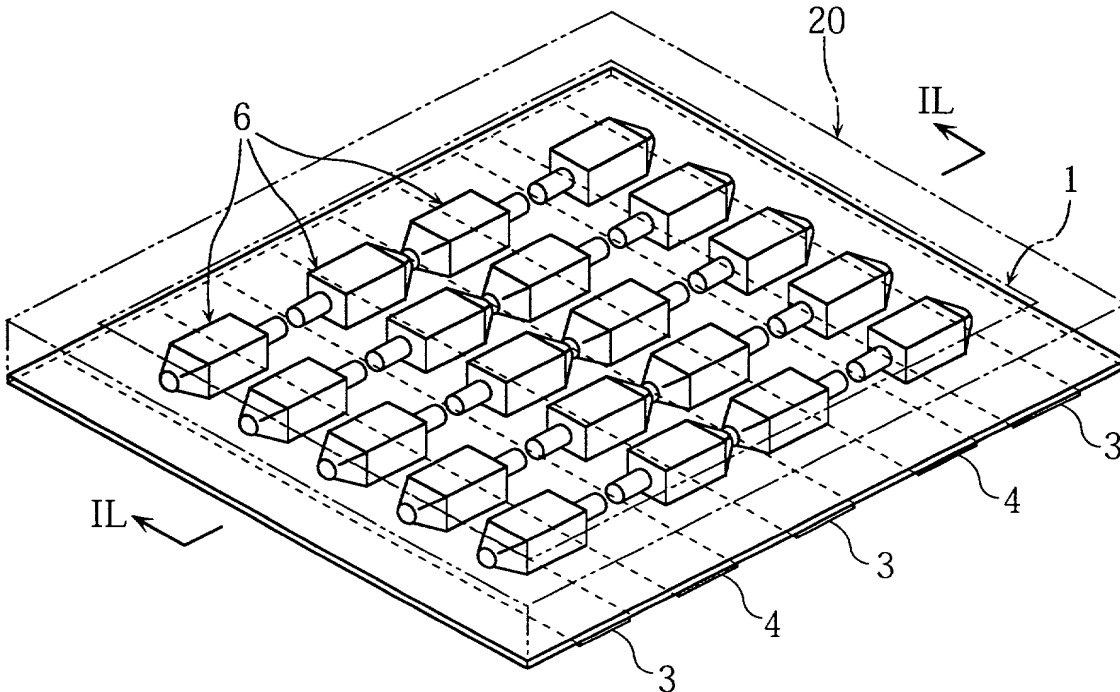


FIG. 48



23/73

FIG. 49

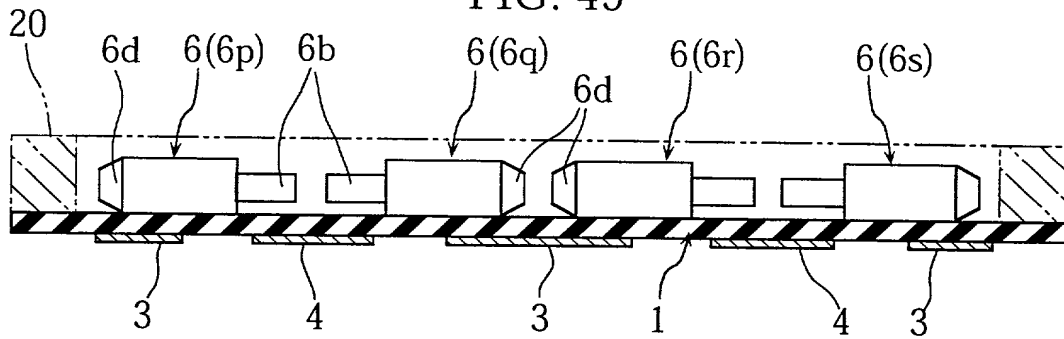


FIG. 50

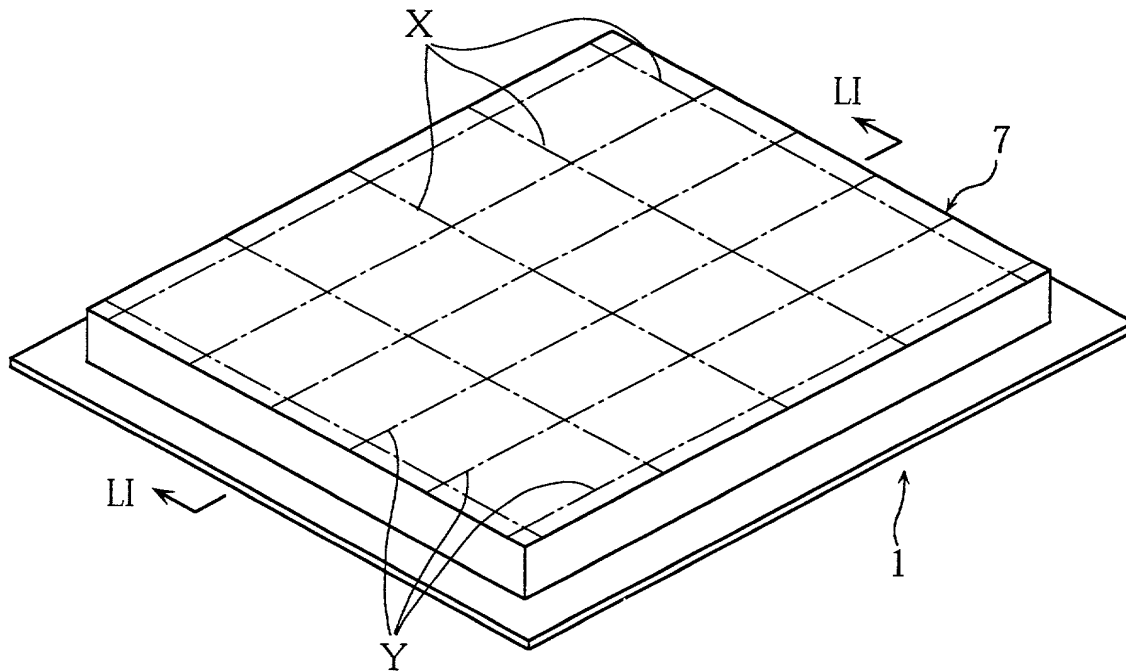
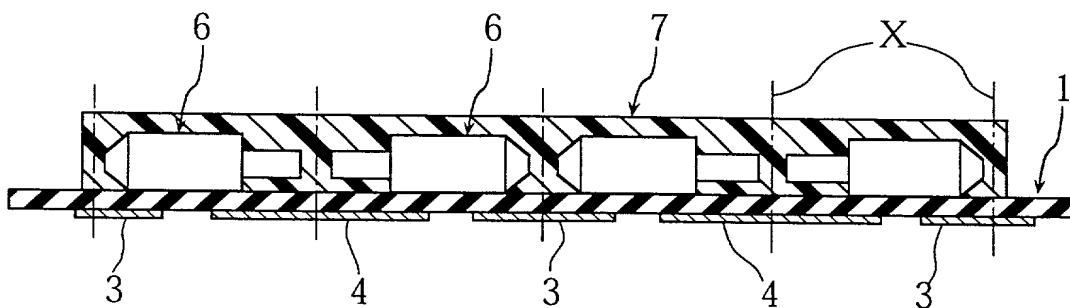


FIG. 51



24/73

FIG. 52

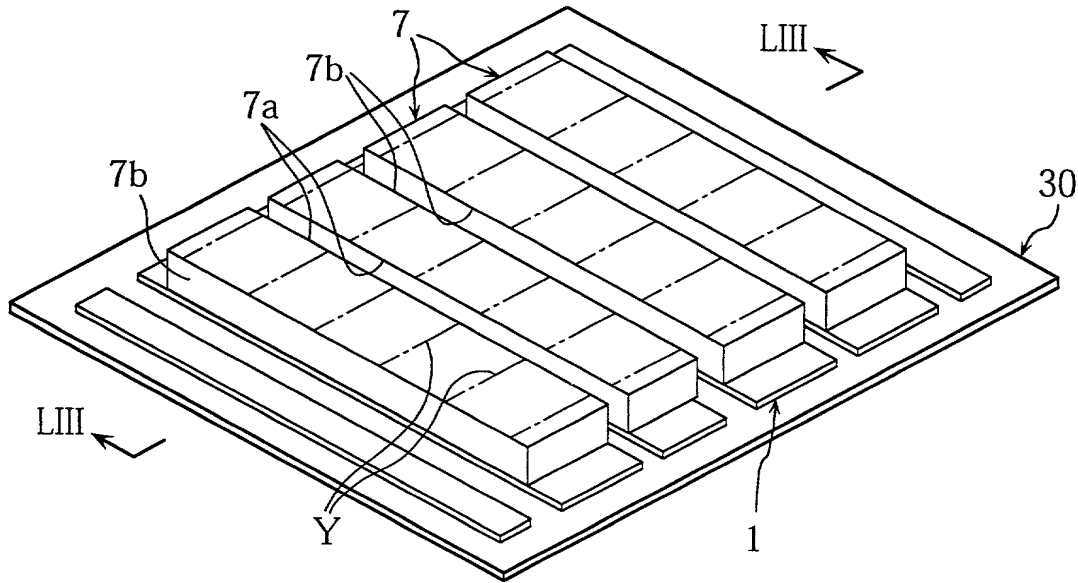
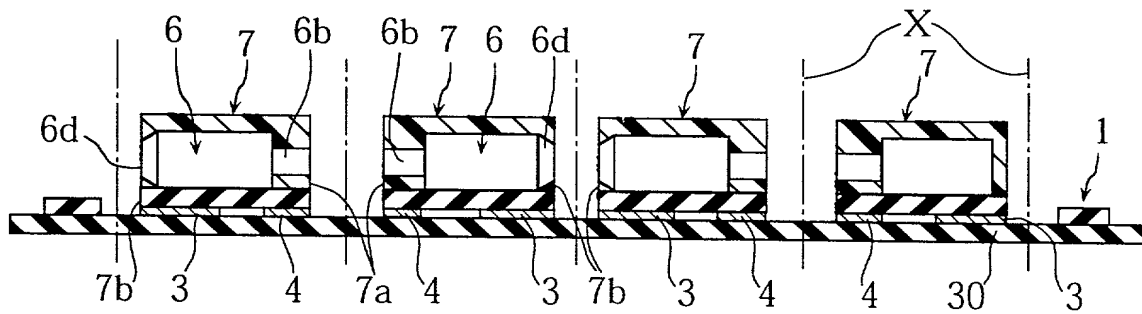


FIG. 53





25/73

FIG. 54

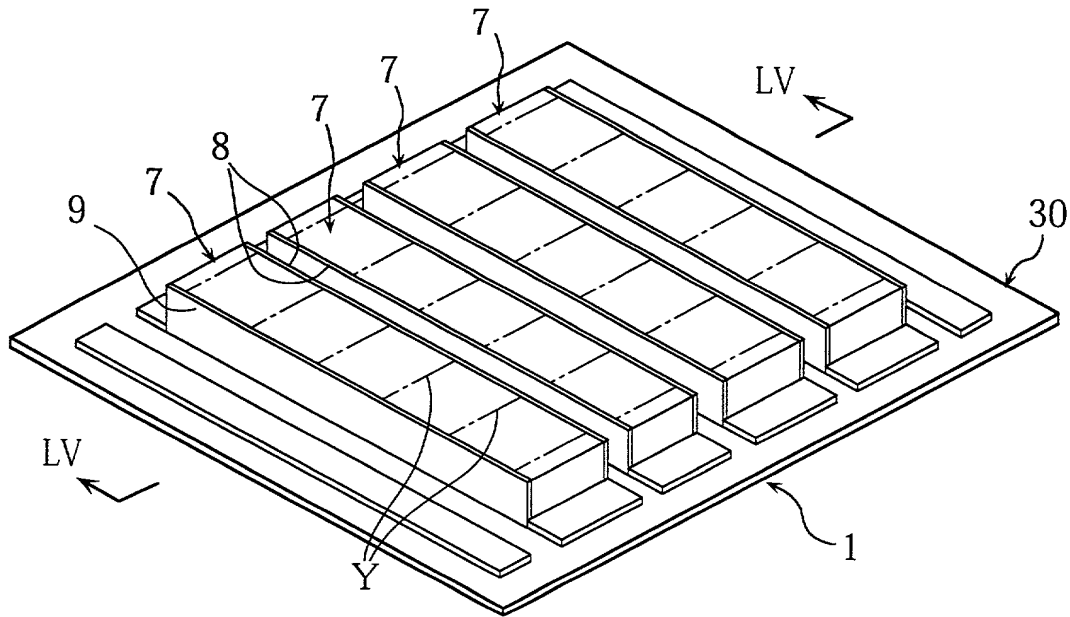
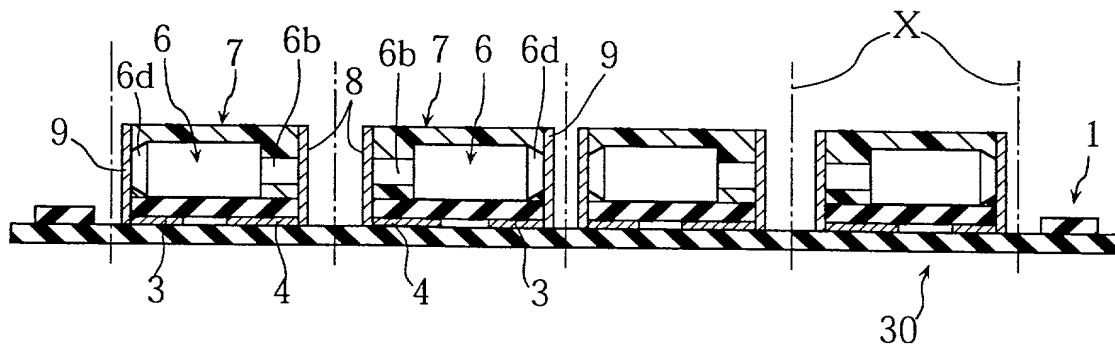


FIG. 55



26/73

FIG. 56

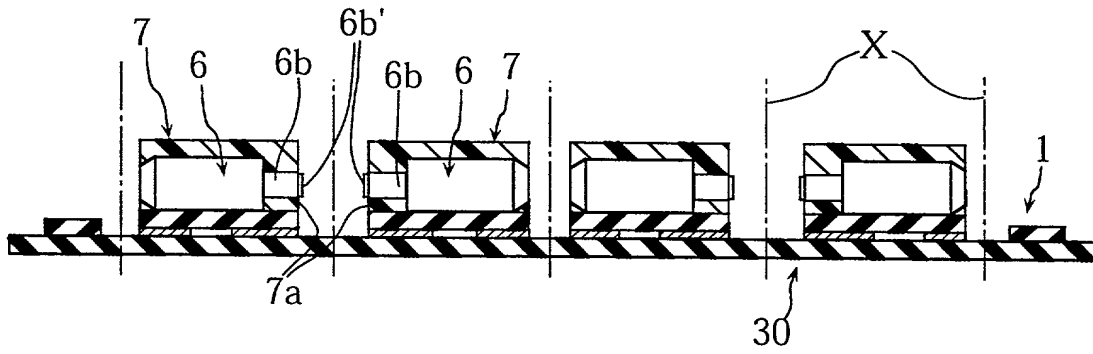
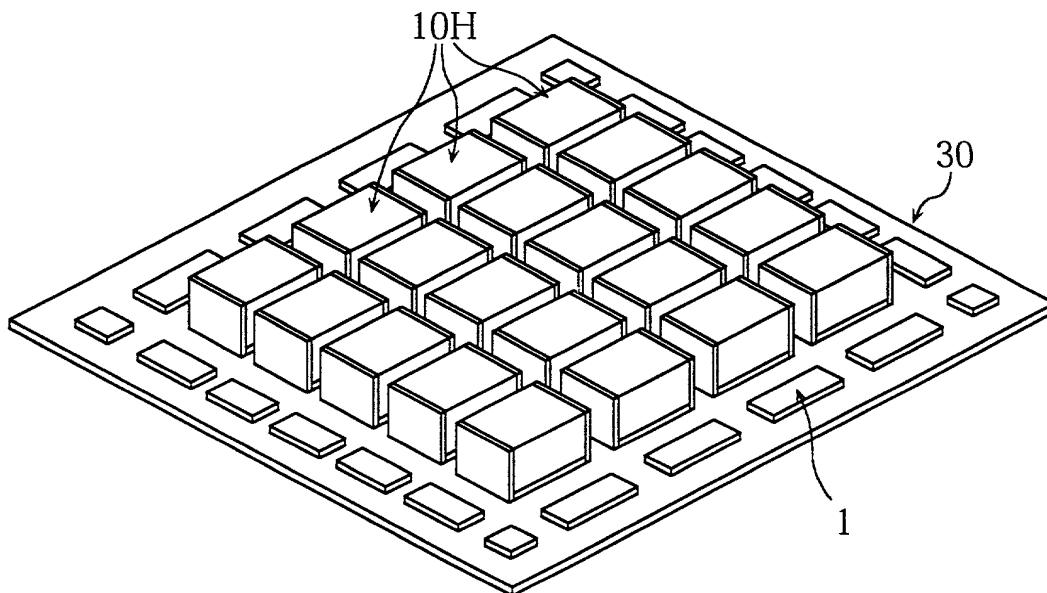


FIG. 57



A detailed cross-sectional diagram of a semiconductor device. It shows a rectangular substrate 6 with a central rectangular cavity 10H. The cavity is outlined with a dashed line. Various layers and components are labeled: 6a is the top surface layer; 6b and 6b' are side wall layers; 6d is a bottom layer adjacent to the cavity; 17 is a top conductive or insulating layer; 17a and 17b are specific regions of layer 17; 18 is a bottom layer; 19 is a side wall layer; T indicates a thickness dimension; 11 and 13 are base layers; 14 is a contact pad; H1 is a height dimension; LX indicates a lateral direction; and 10H is the central cavity.

28/73

FIG. 60

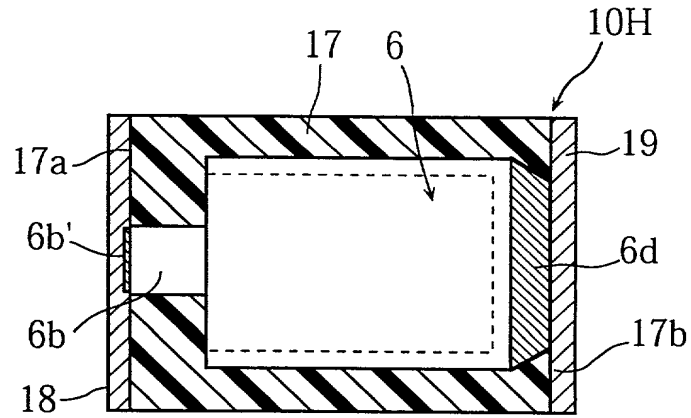


FIG. 61

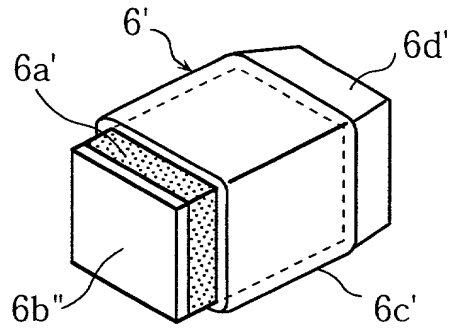
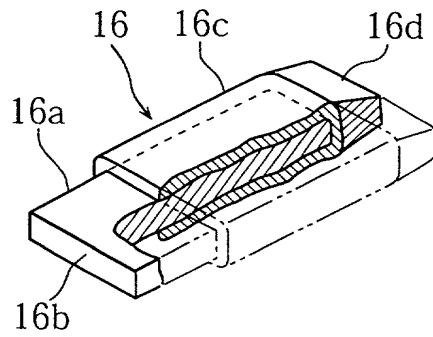


FIG. 62



29/73

FIG. 63

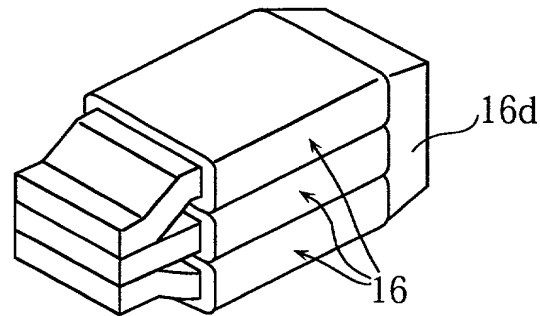


FIG. 64

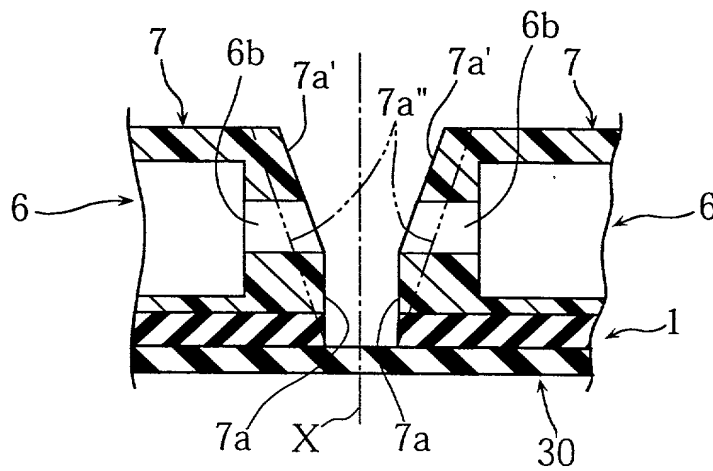


Fig. 10H' is a cross-sectional view of a semiconductor device. It shows a central rectangular region (6) surrounded by a dashed-line boundary (17). This central region is enclosed by a thick, hatched layer (19). The hatched layer is further surrounded by a layer (17b) and a layer (17a'). The device is mounted on a substrate (11) via solder bumps (12, 13). A layer (18) is located between the hatched layer (19) and the substrate (11). A layer (17a'') is also indicated on the left side of the device.

31/73

FIG. 67

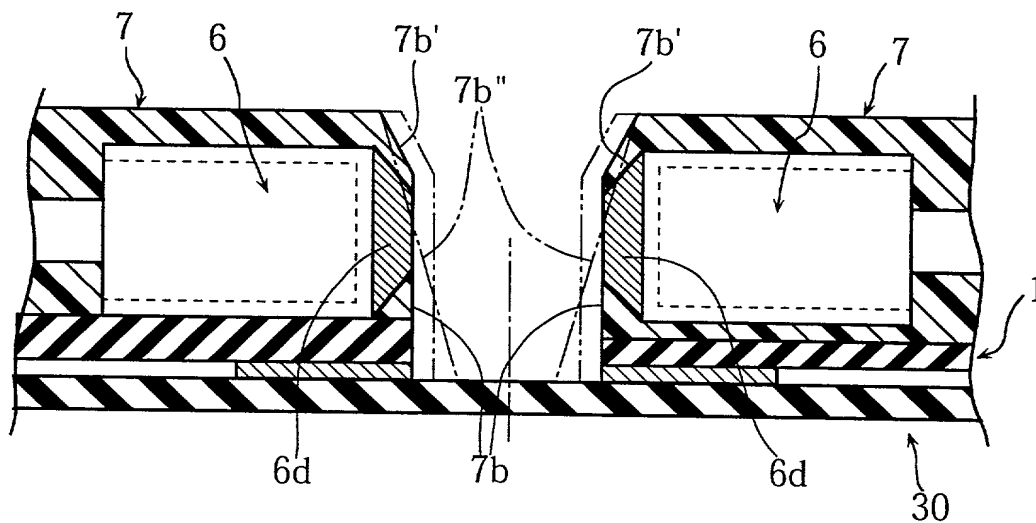
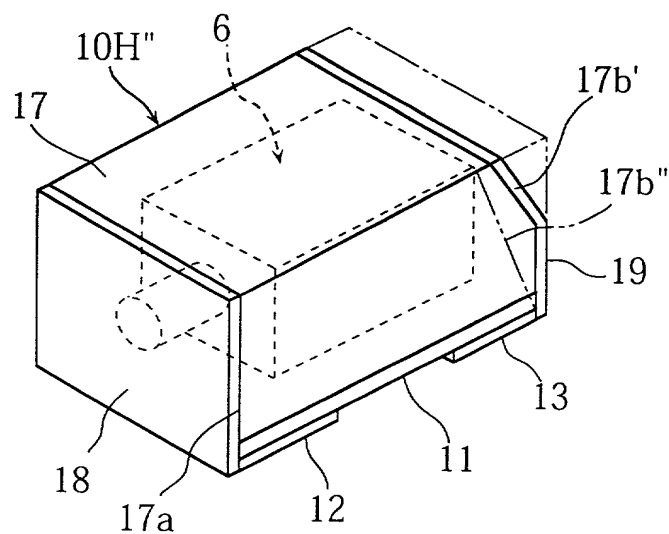


FIG. 68



32/73

FIG. 69

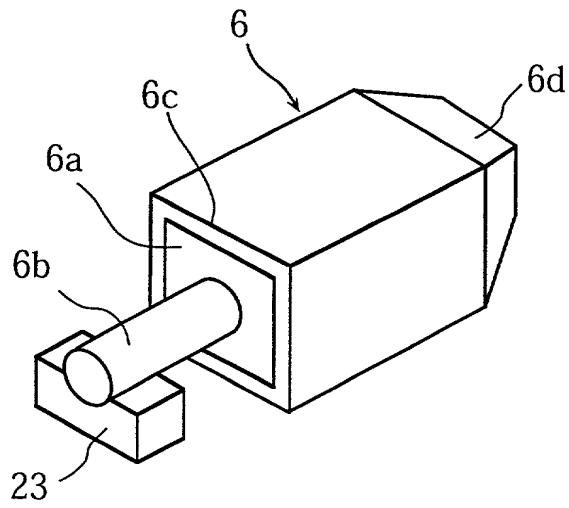
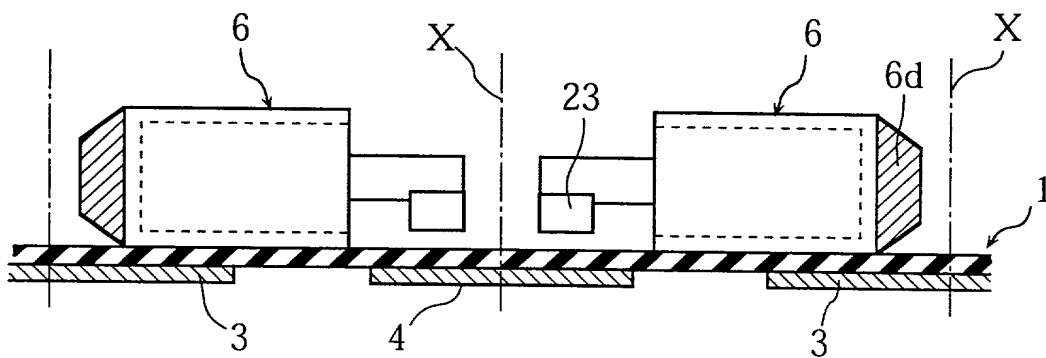


FIG. 70





33/73

FIG. 71

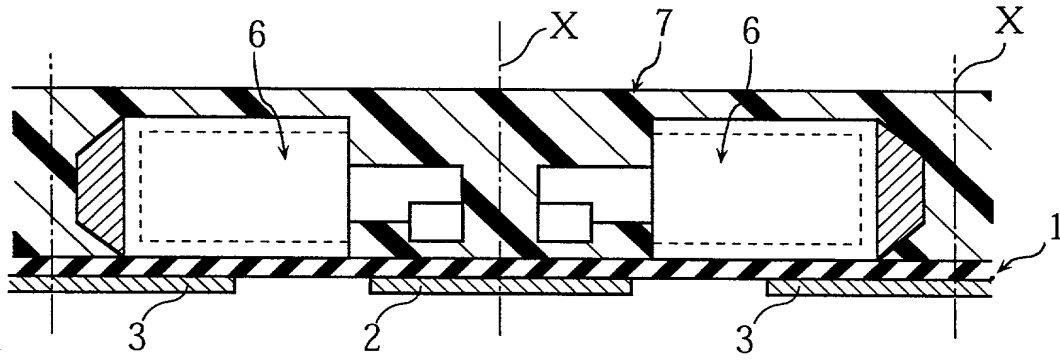
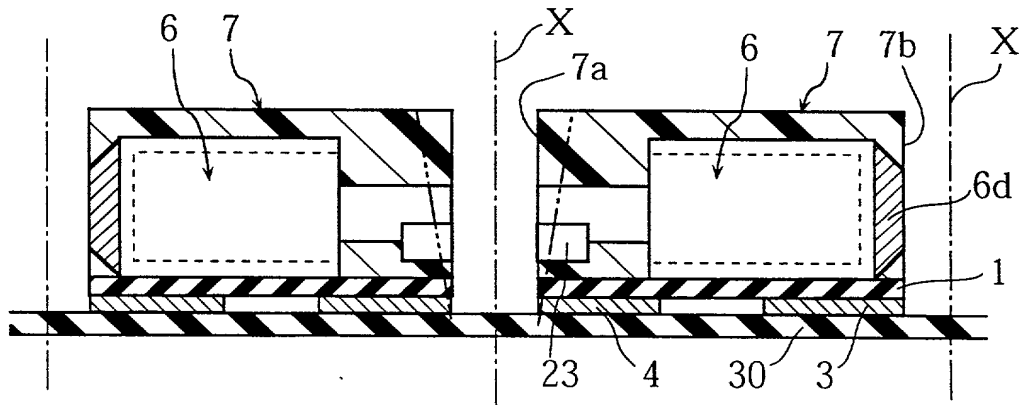


FIG. 72



10005944-110901

34/73

FIG. 73

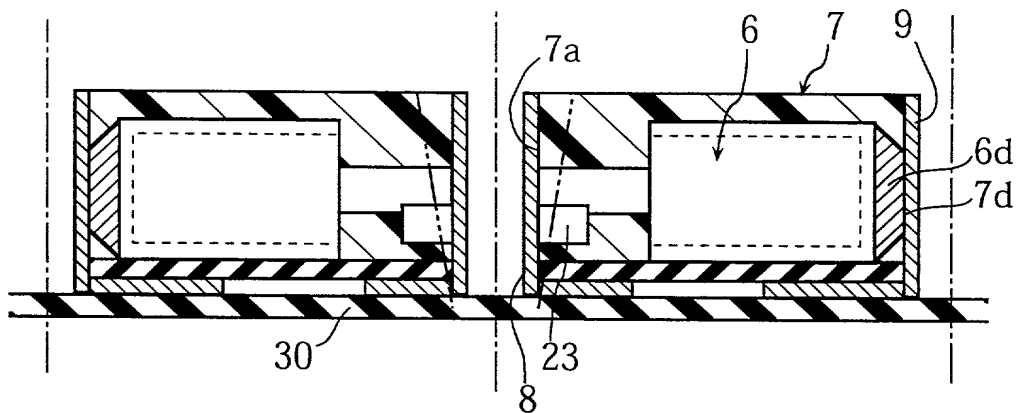


FIG. 74

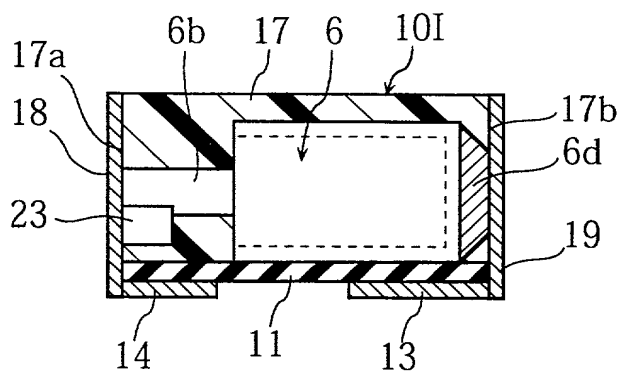
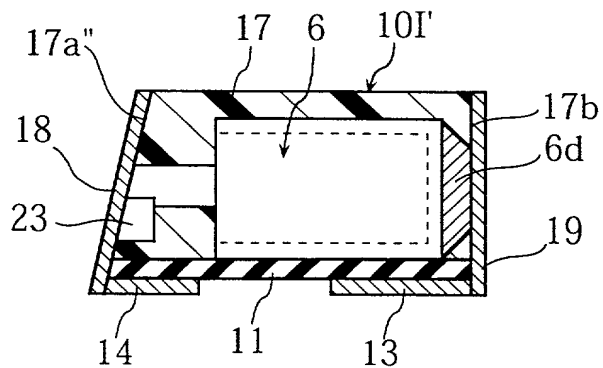


FIG. 75



106011-4663001

35/73

FIG. 76

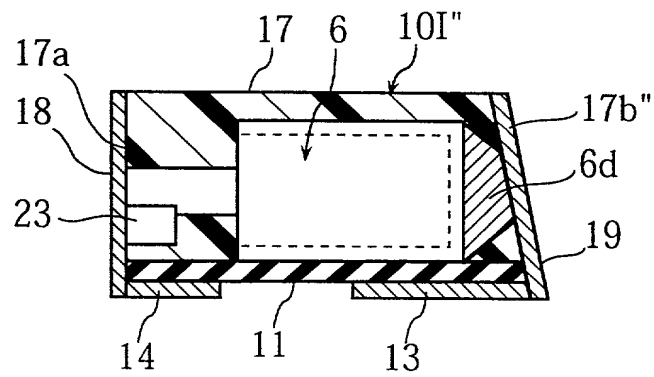
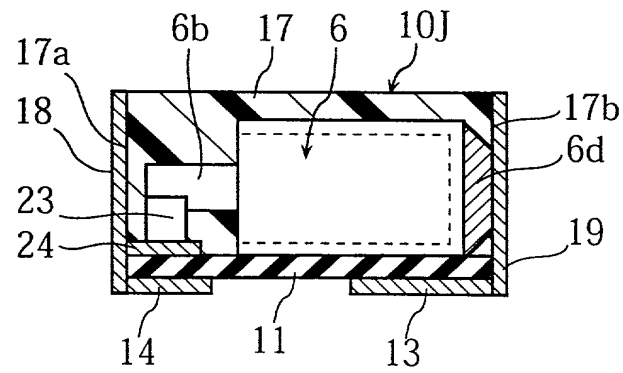


FIG. 77



36/73

FIG. 78

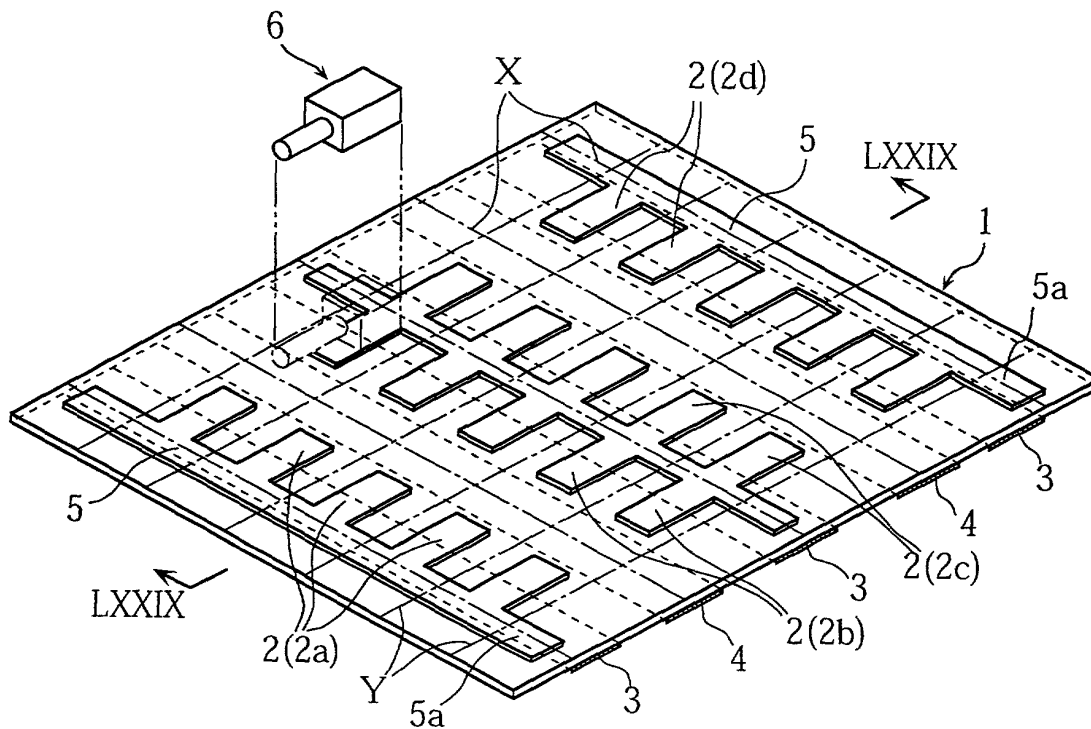


FIG. 79

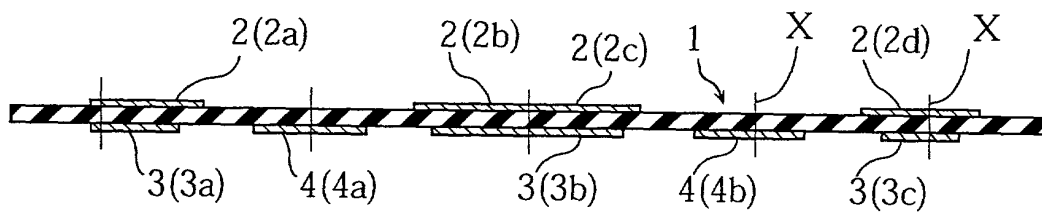
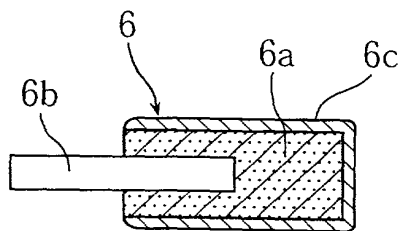
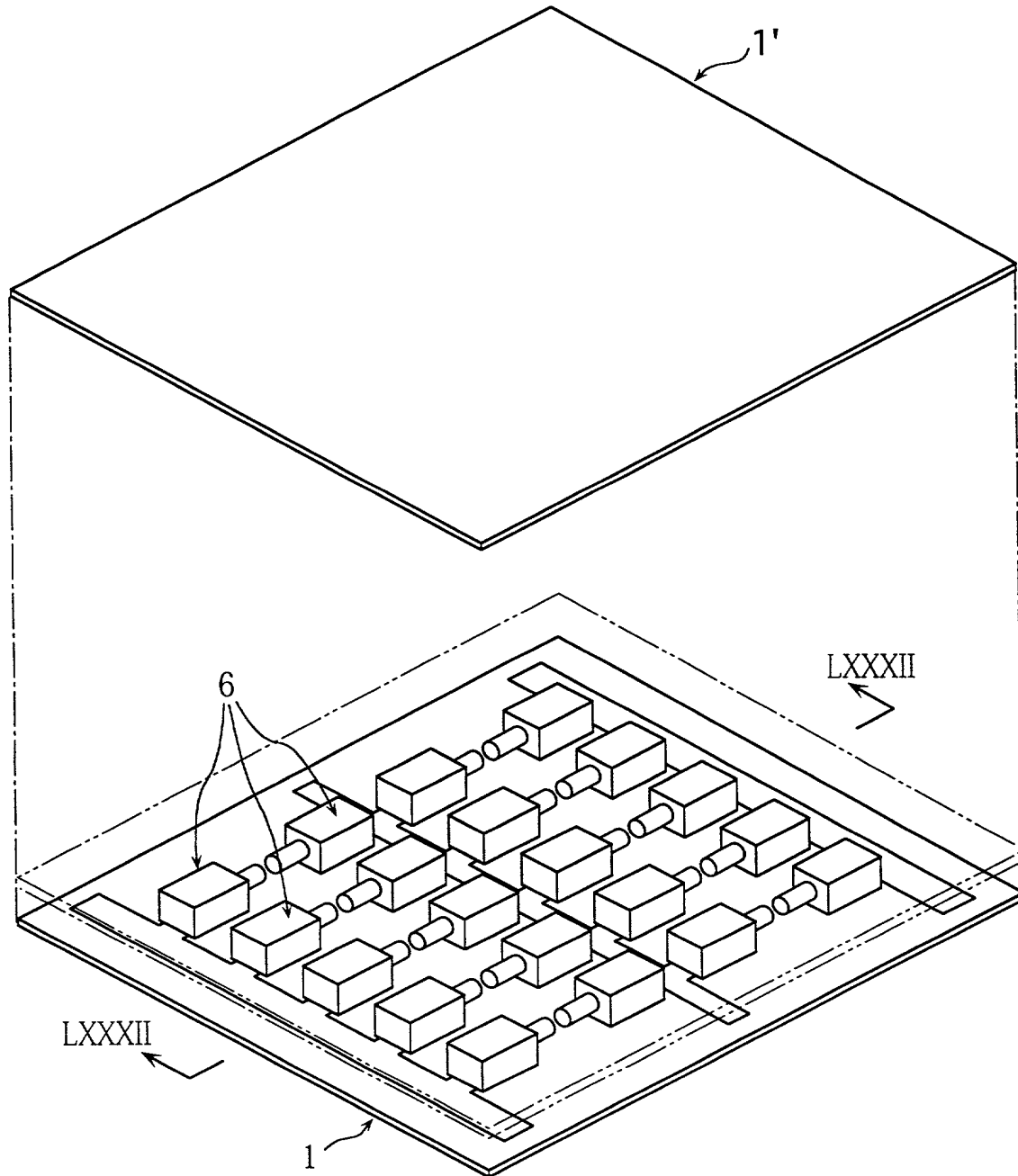


FIG. 80



37/73

FIG. 81



38/73

FIG. 82

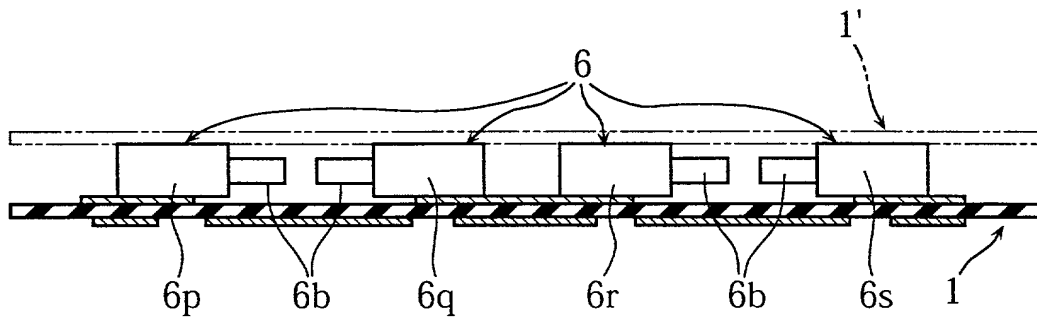
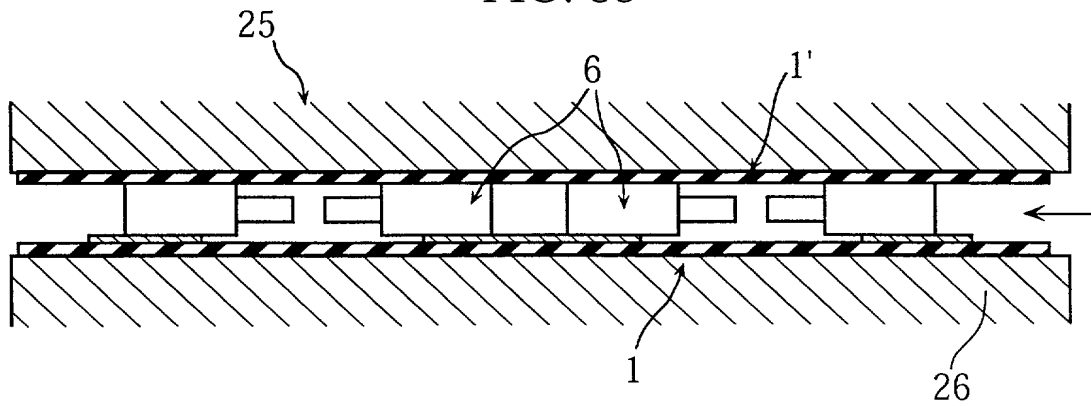


FIG. 83



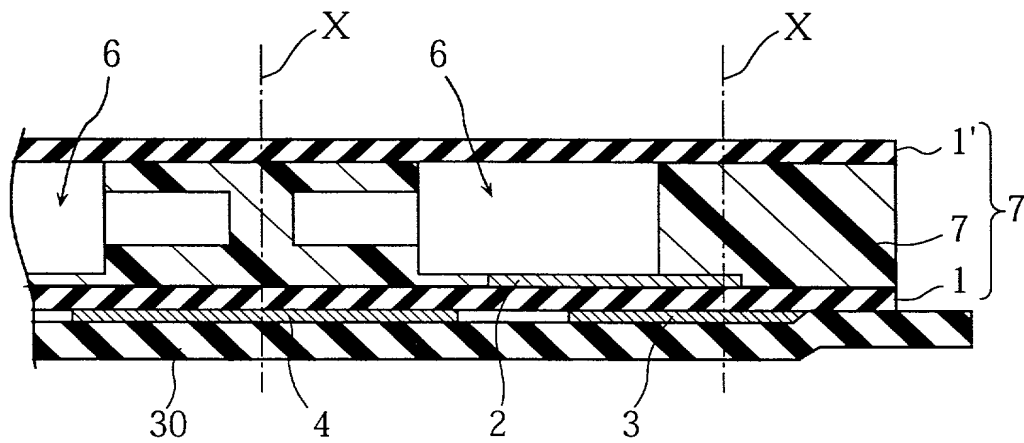


FIG. 86

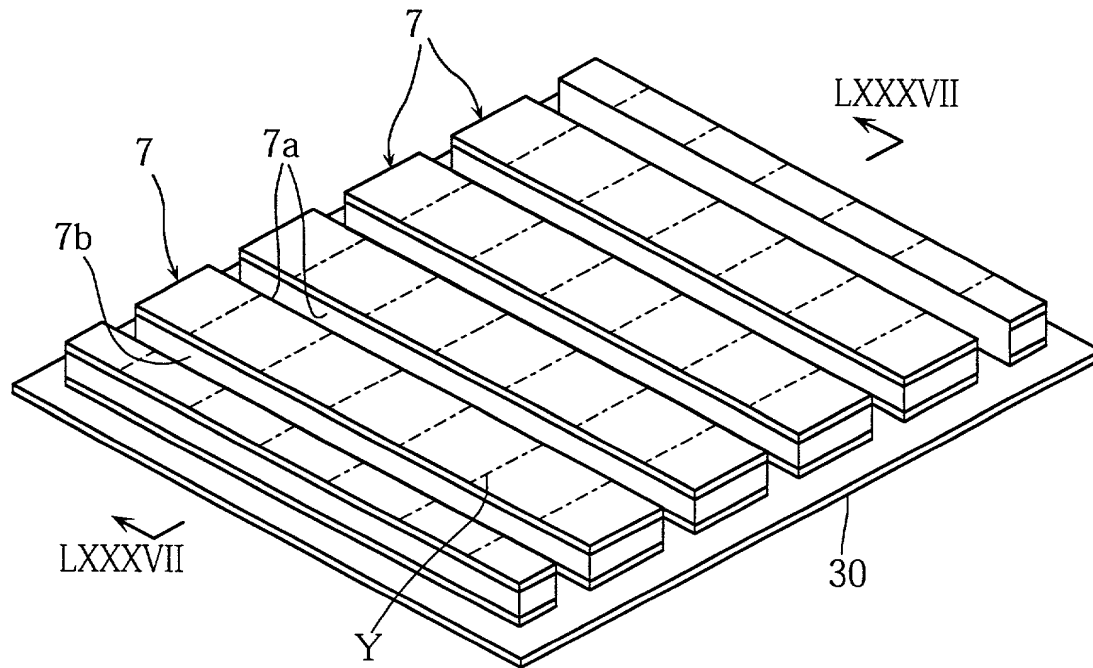
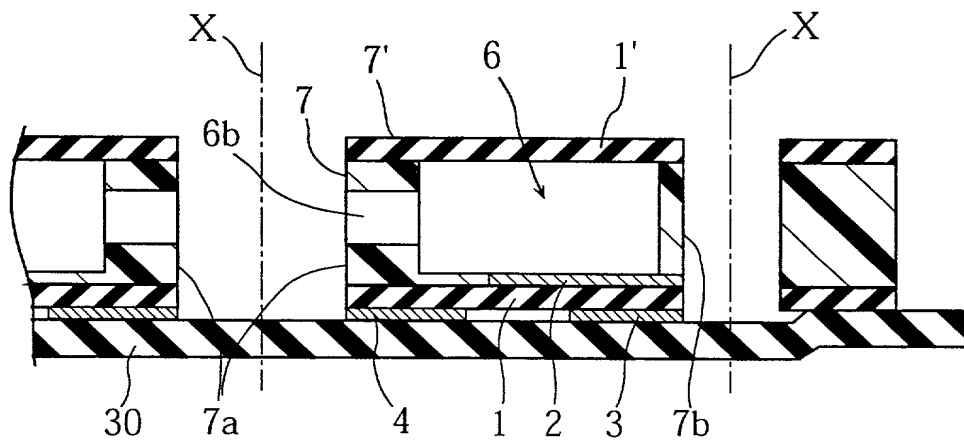


FIG. 87





41/73

FIG. 88

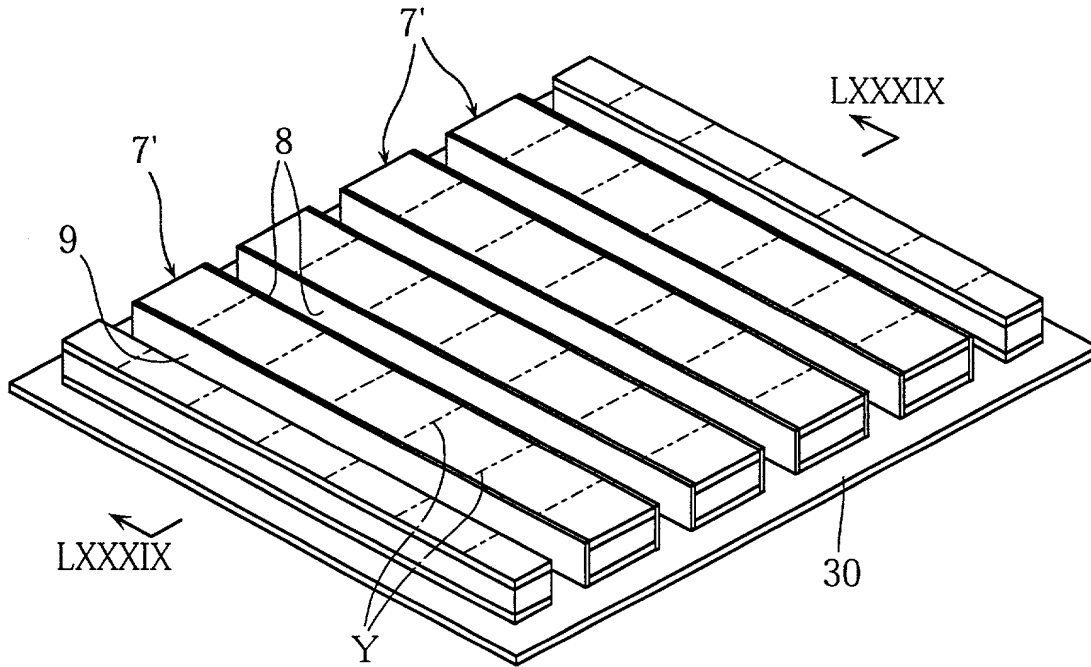
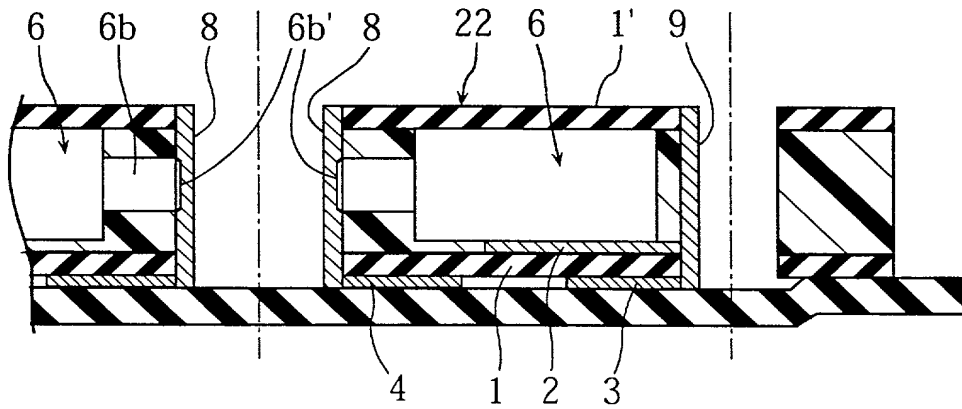


FIG. 89



[illegible]

Figure 1 is a perspective view of a 3D array of memory cells. The array consists of a grid of rectangular blocks (memory cells) arranged in rows and columns. A label '10K' with arrows points to several blocks in the top row. A label '30' with a line points to the base of the array.

FIG. 92

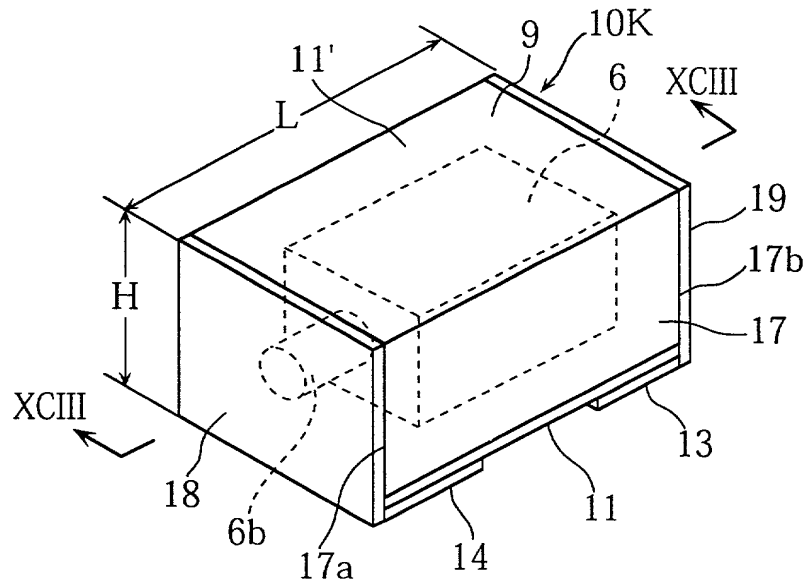
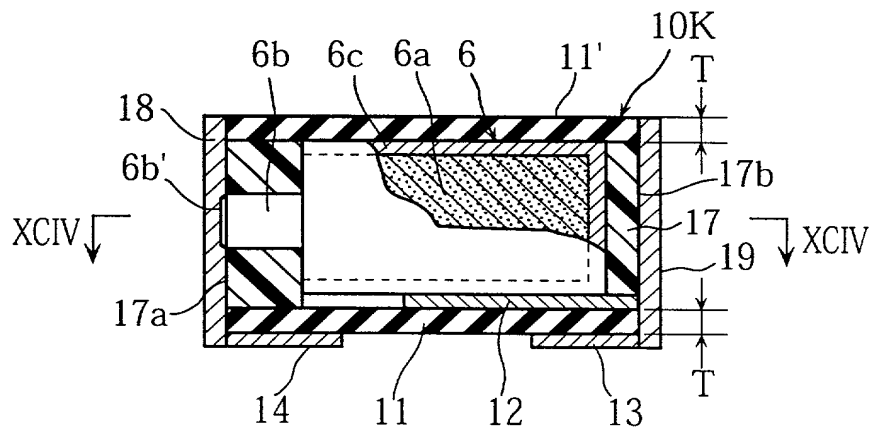


FIG. 93



44/73

FIG. 94

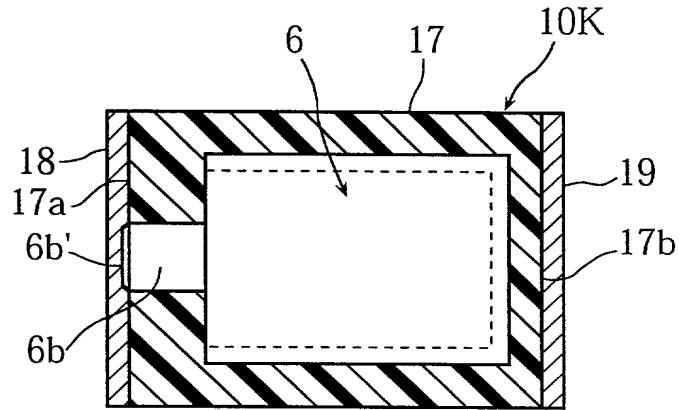
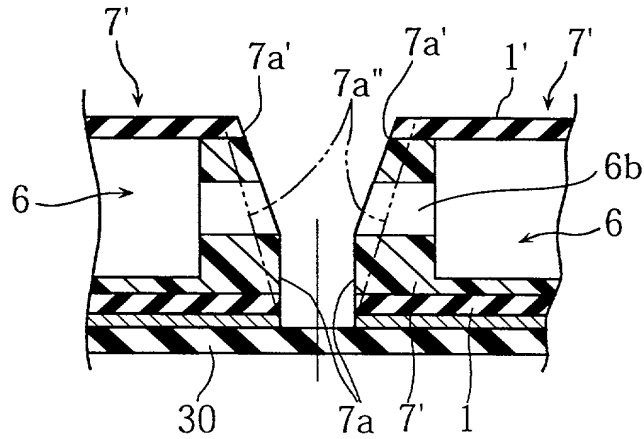


FIG. 95



45/73

FIG. 96

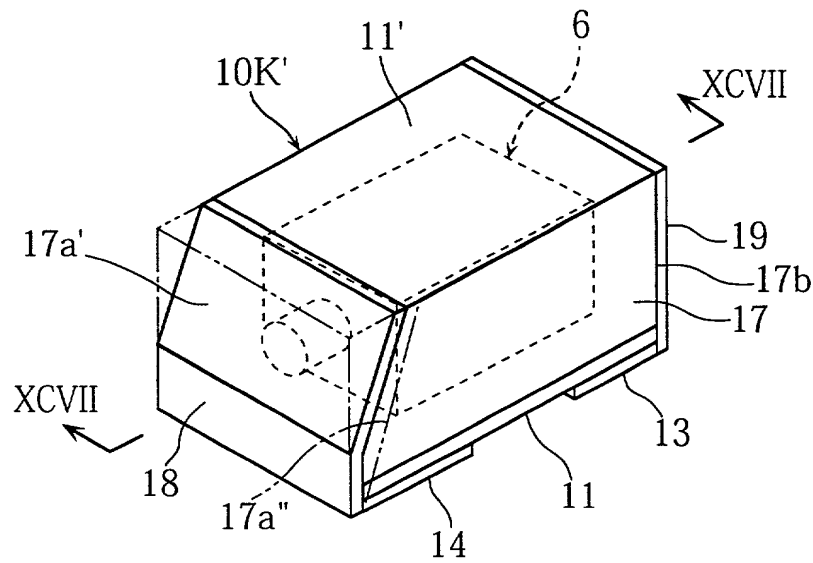
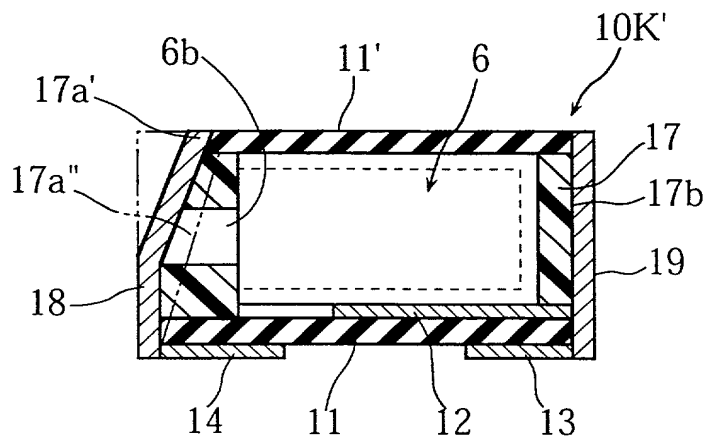


FIG. 97



10008934-110901

FIG. 98

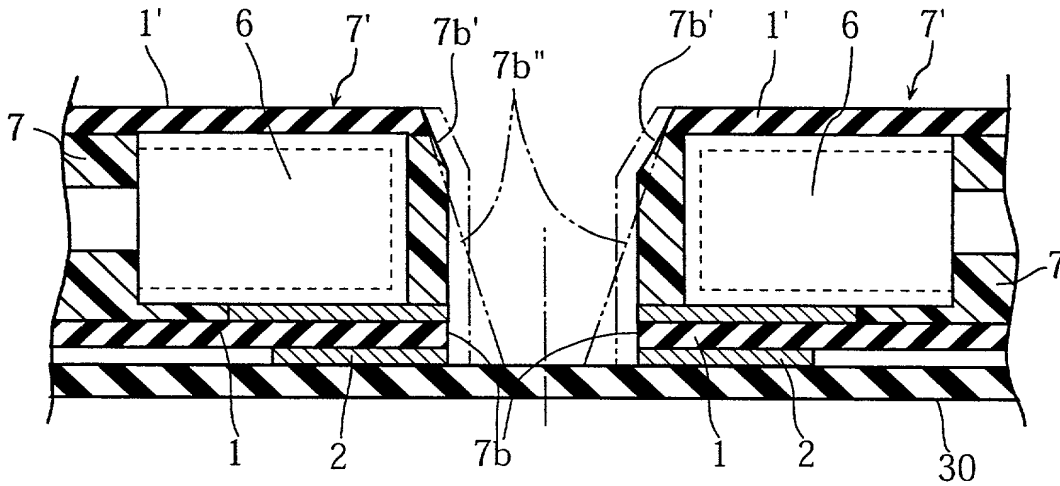
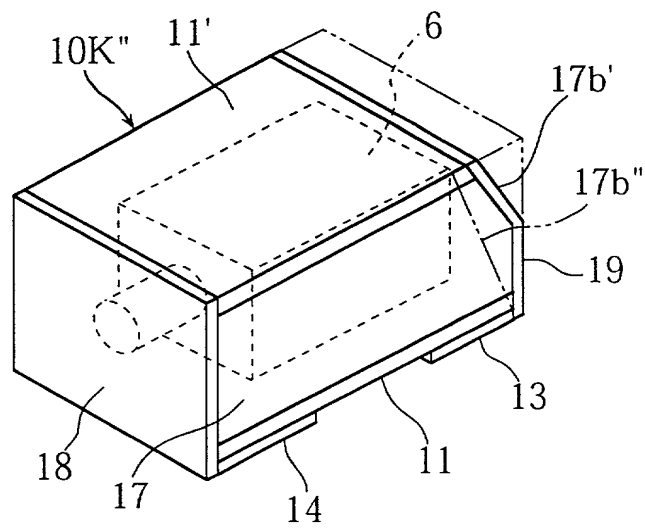


FIG. 99



47/73

FIG. 100

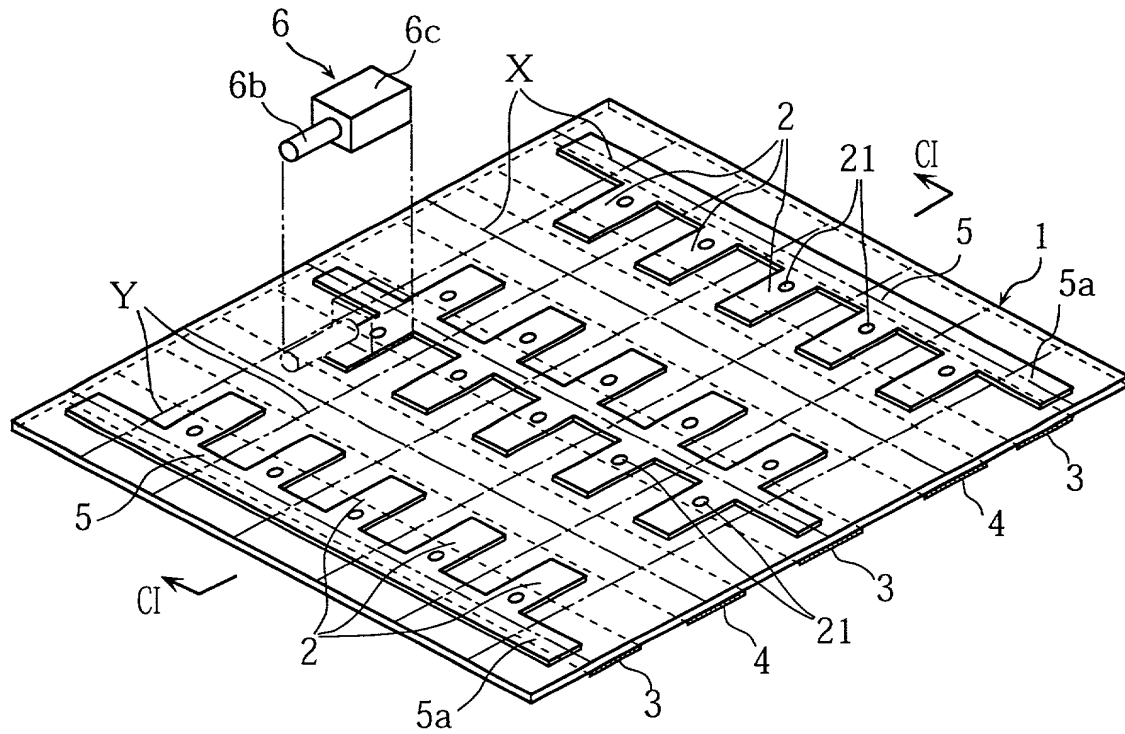
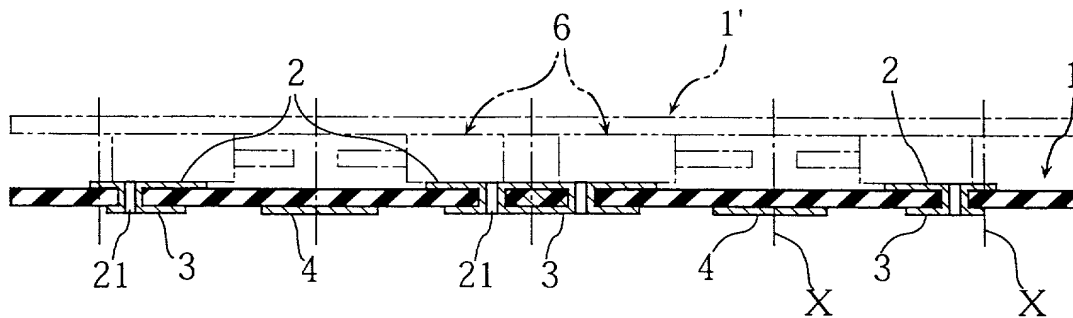


FIG. 101



48/73

FIG. 102

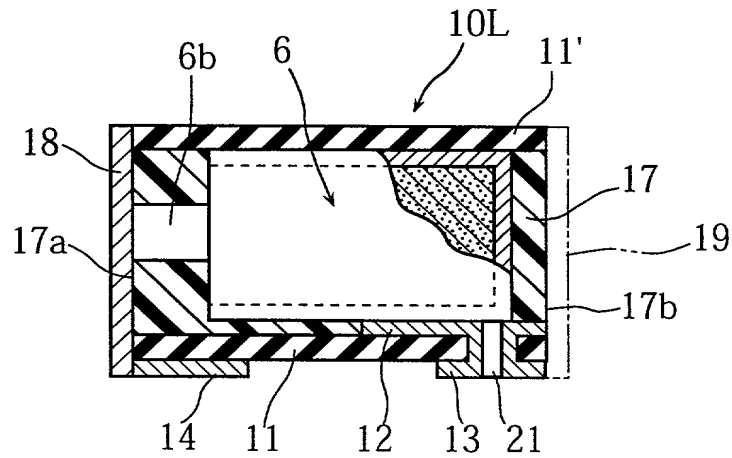
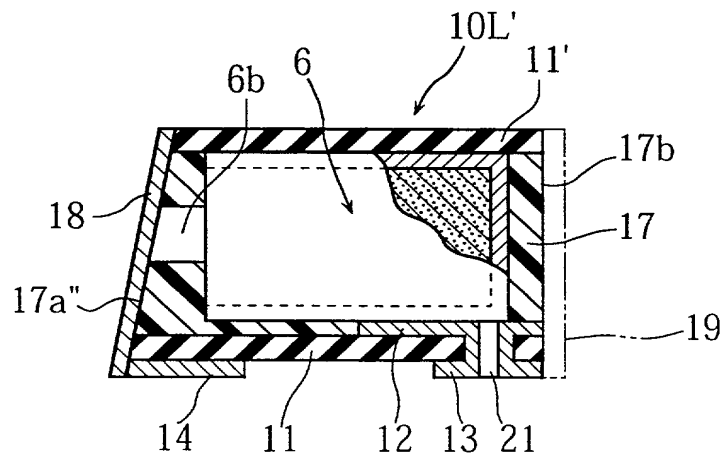


FIG. 103





49/73

FIG. 104

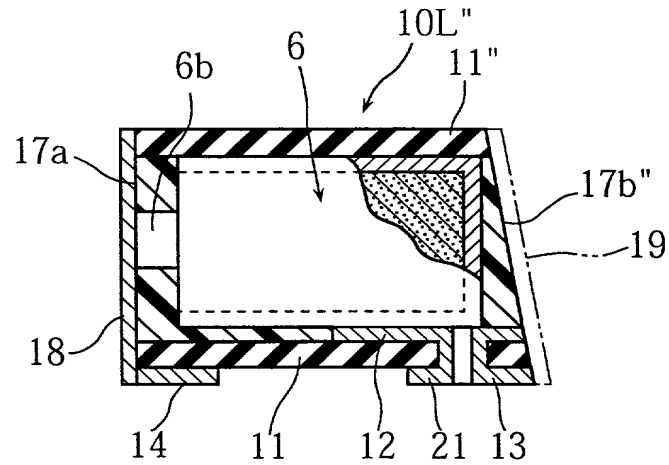


FIG. 105

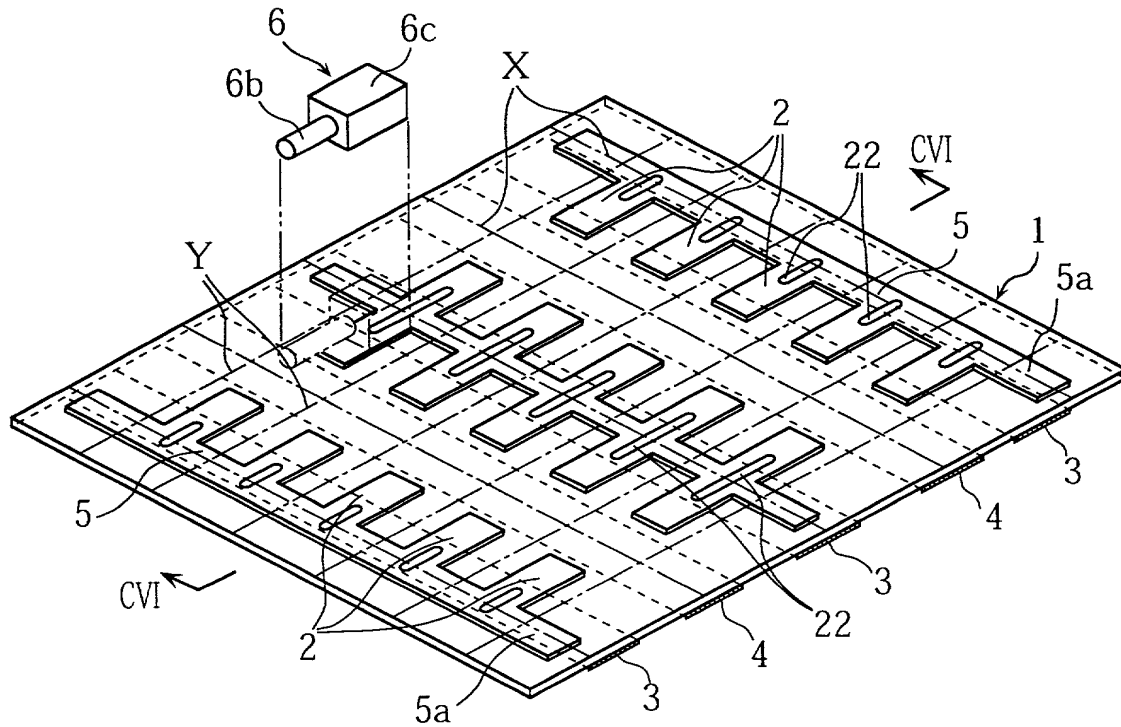


FIG. 106

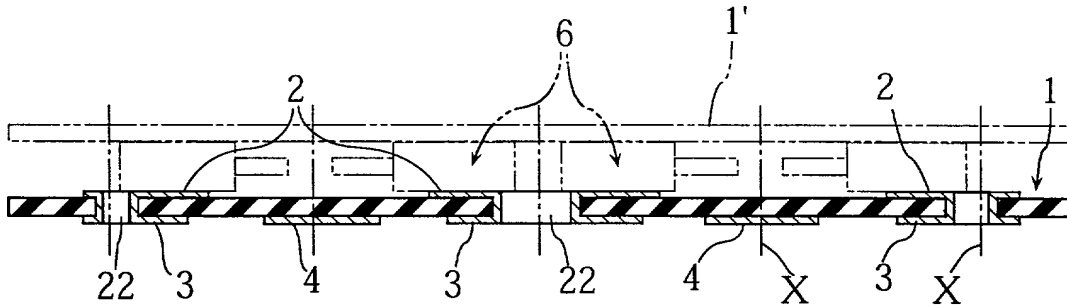


FIG. 107

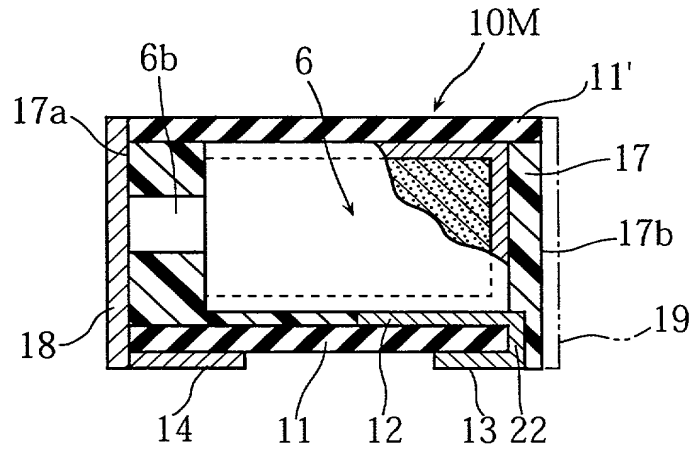
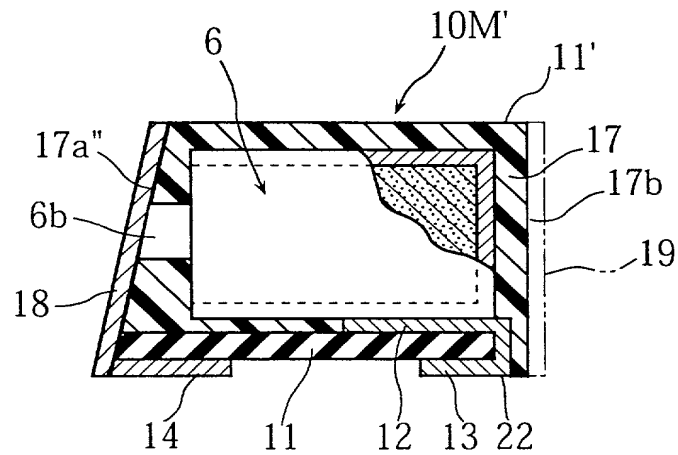


FIG. 108



51/73

FIG. 109

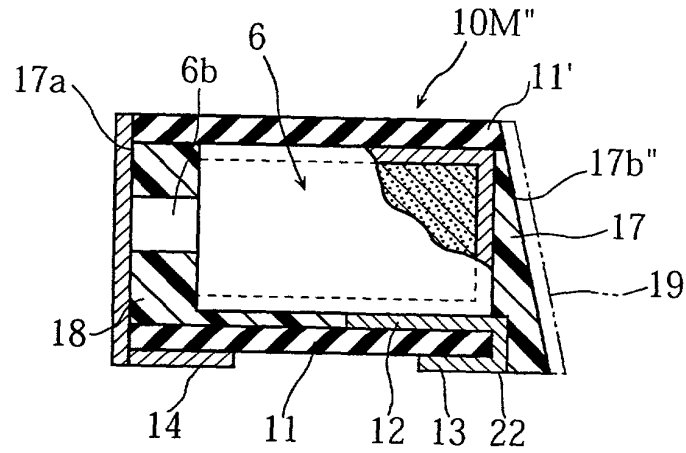


FIG. 110

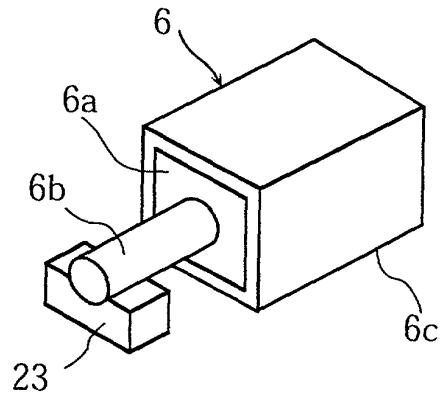
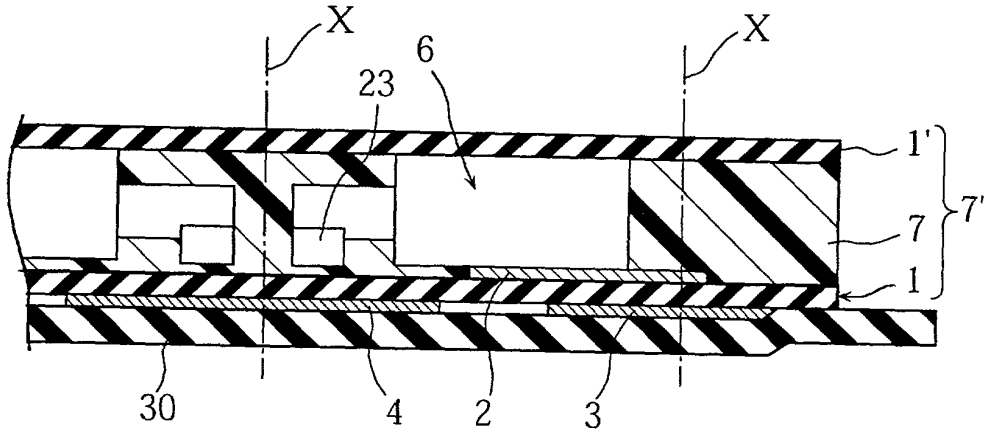


FIG. 111



52/73

FIG. 112

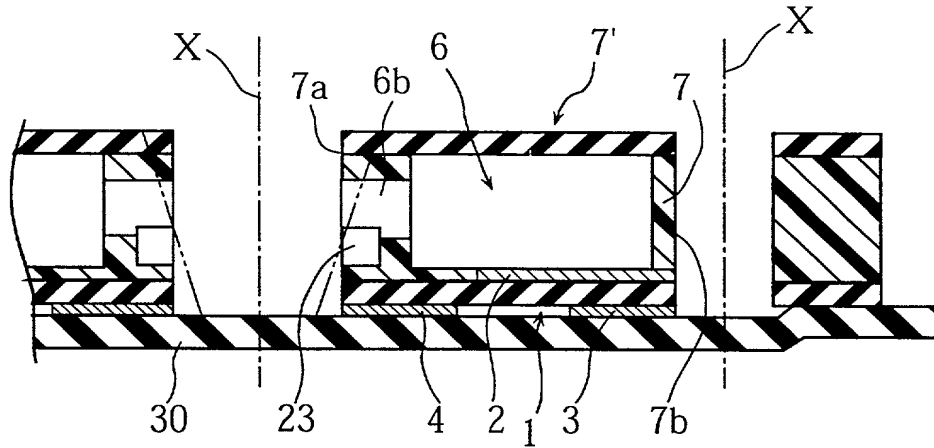


FIG. 113

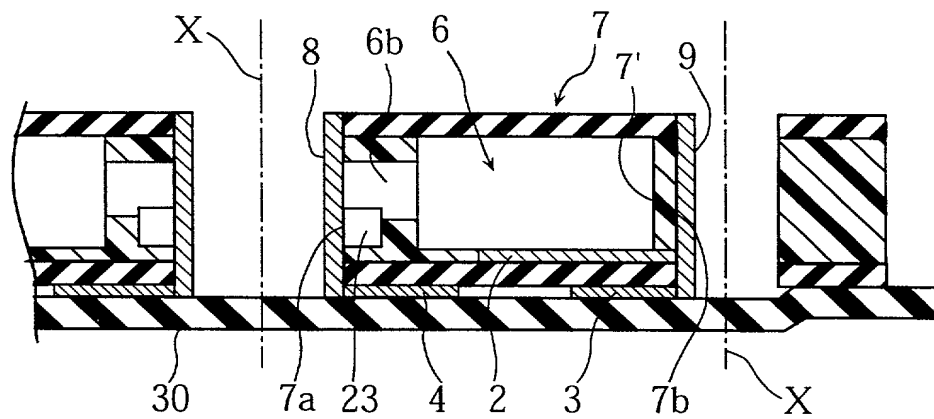
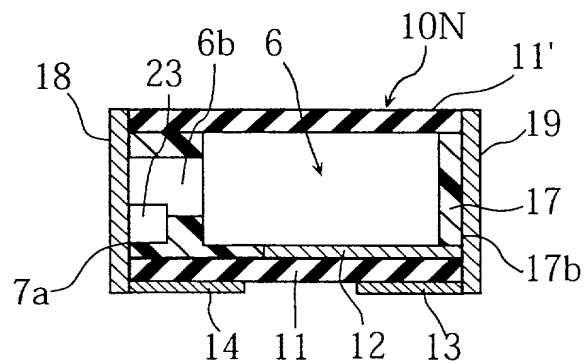


FIG. 114



53/73

FIG. 115

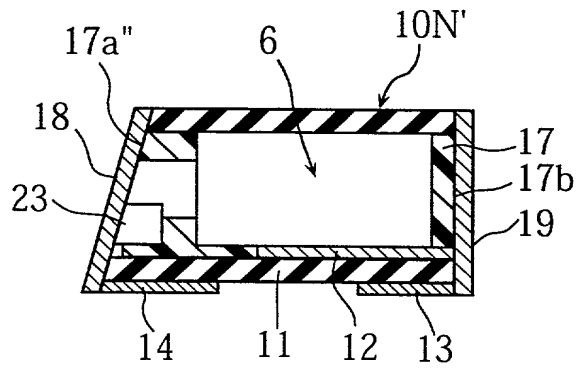
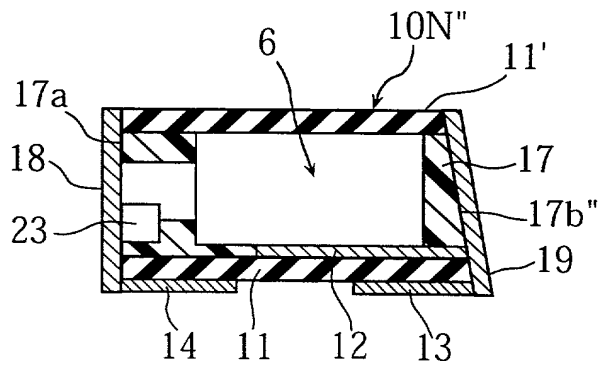


FIG. 116



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FIG. 117

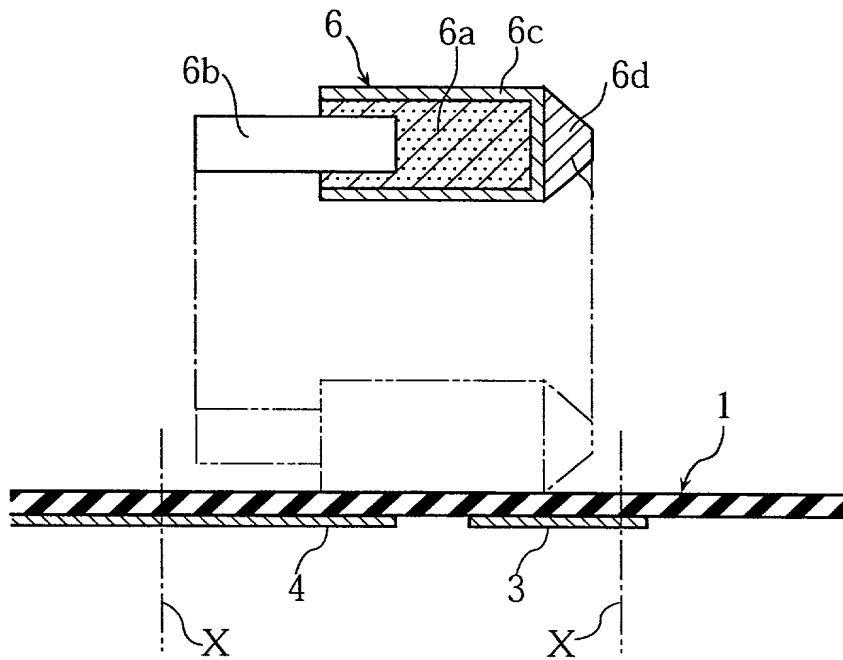
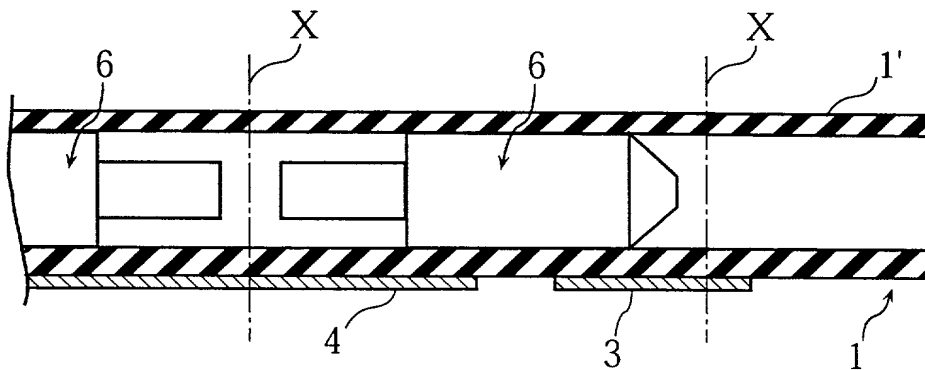


FIG. 118



55/73

FIG. 119

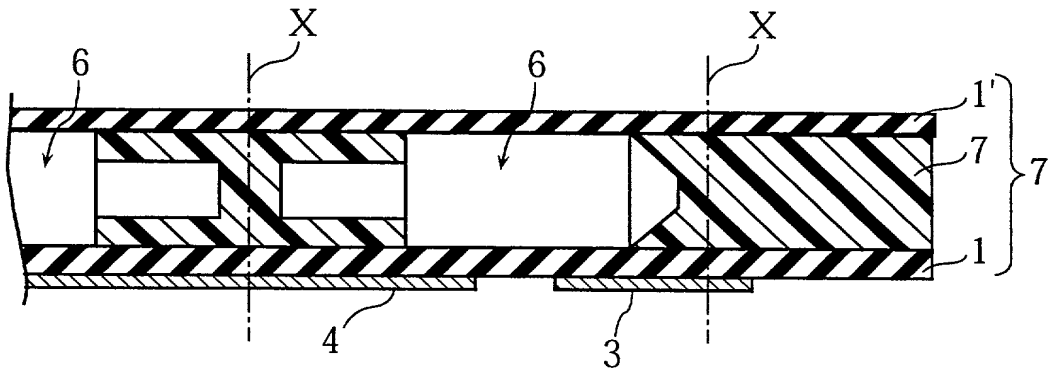
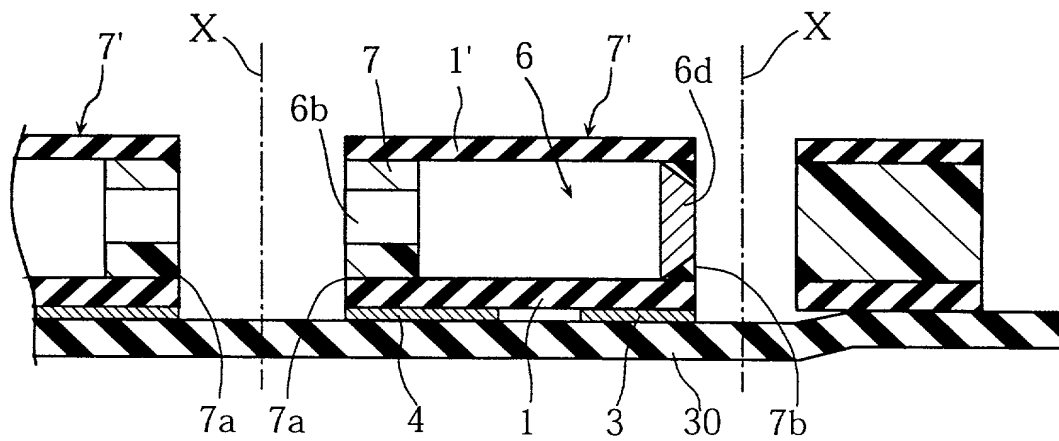


FIG. 120



56/73

FIG. 121

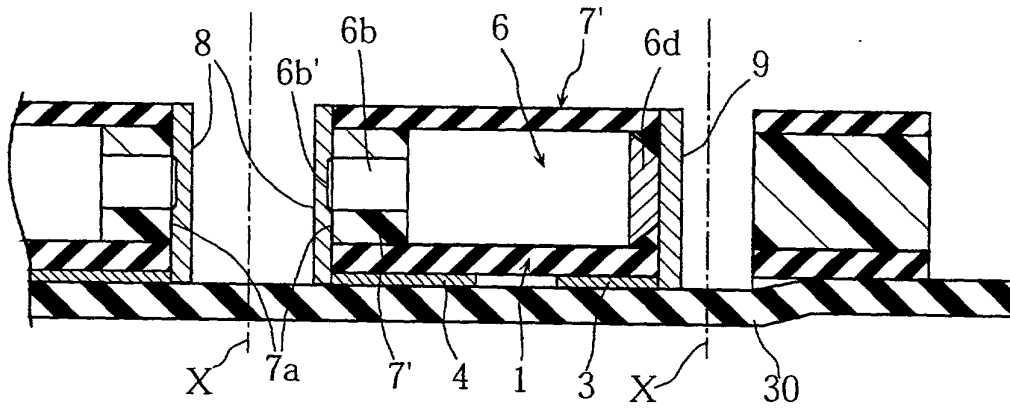
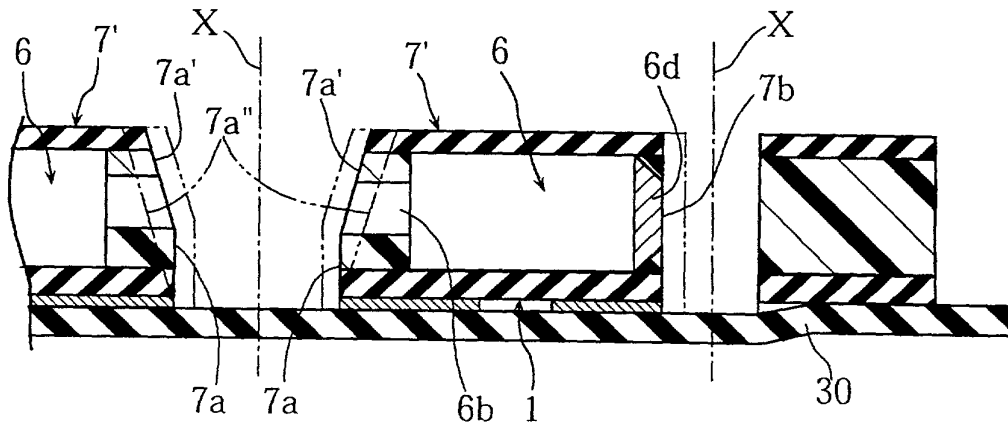
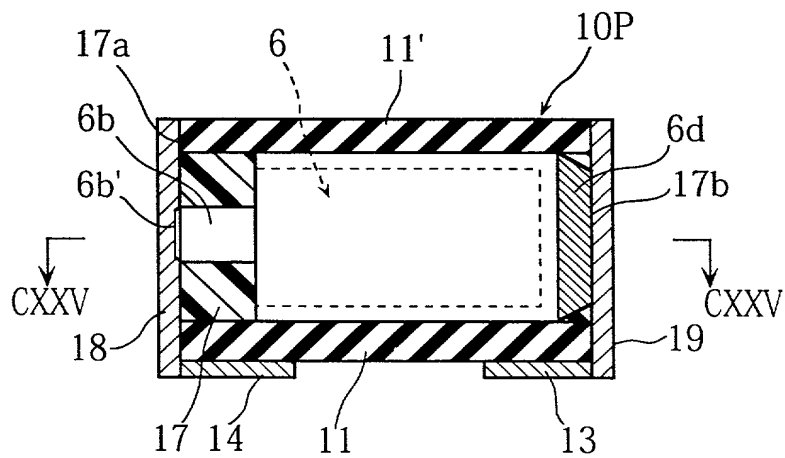


FIG. 122







58/73

FIG. 125

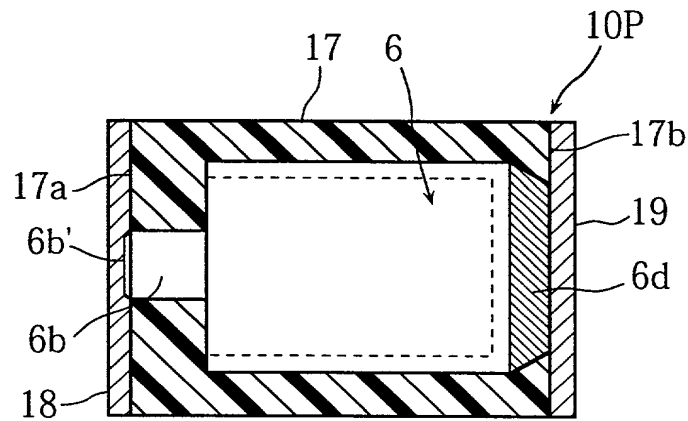


FIG. 126

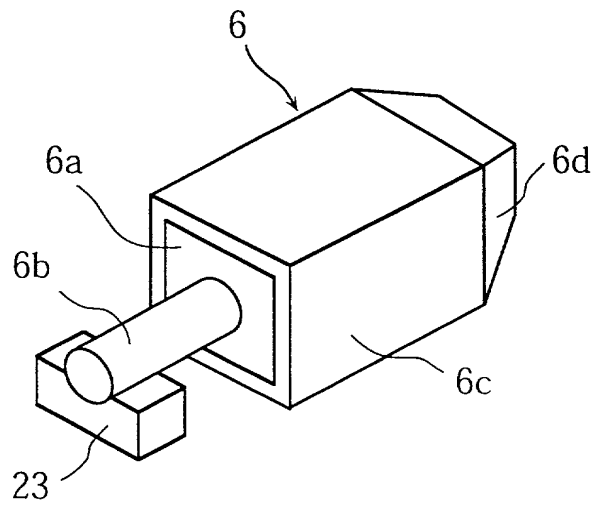


FIG. 127

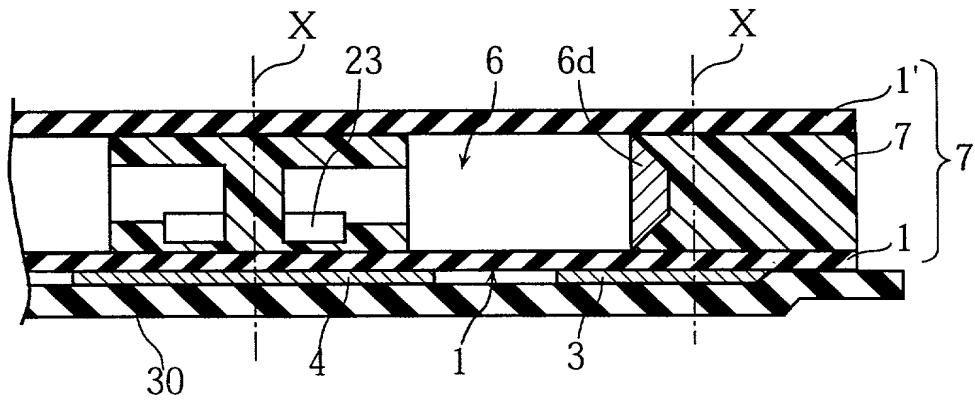
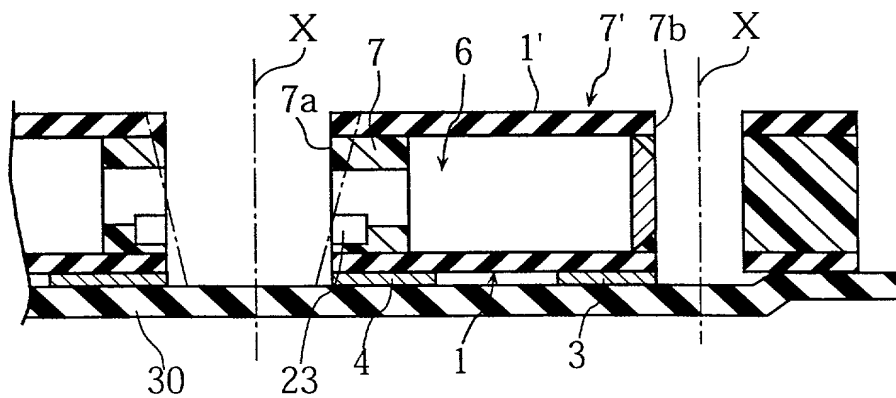


FIG. 128



60/73

FIG. 129

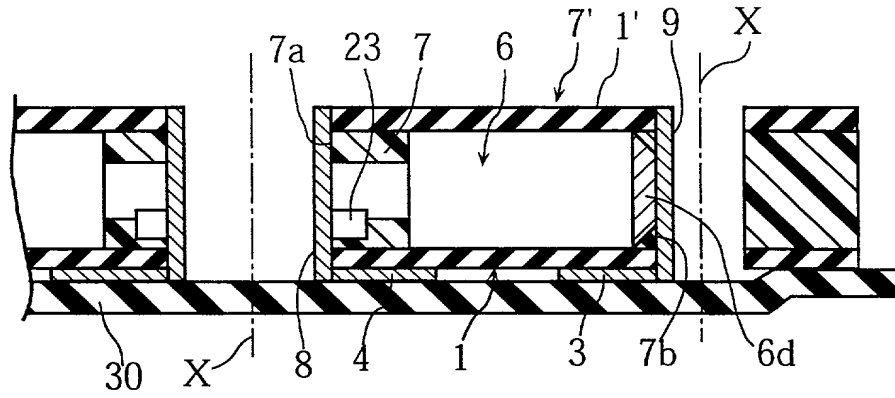


FIG. 130

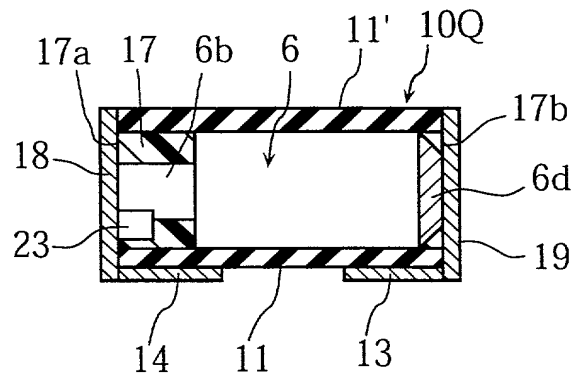
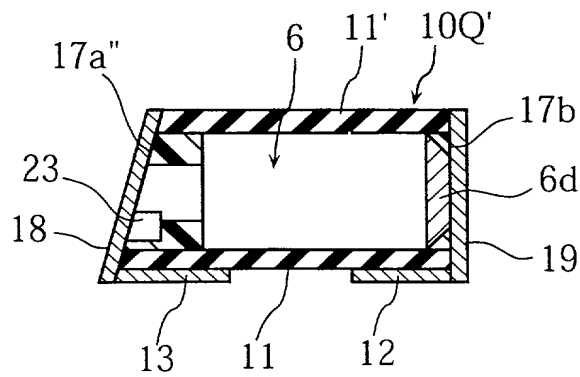


FIG. 131



61/73

FIG. 132

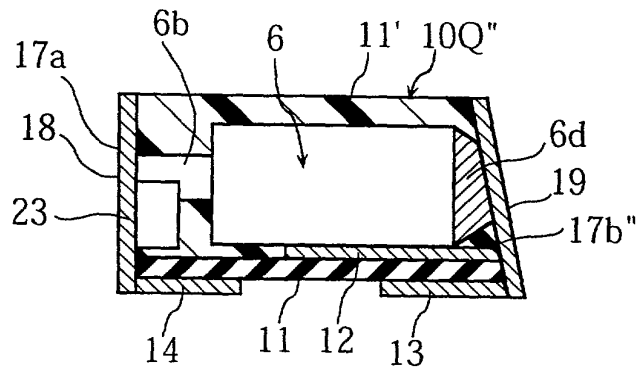
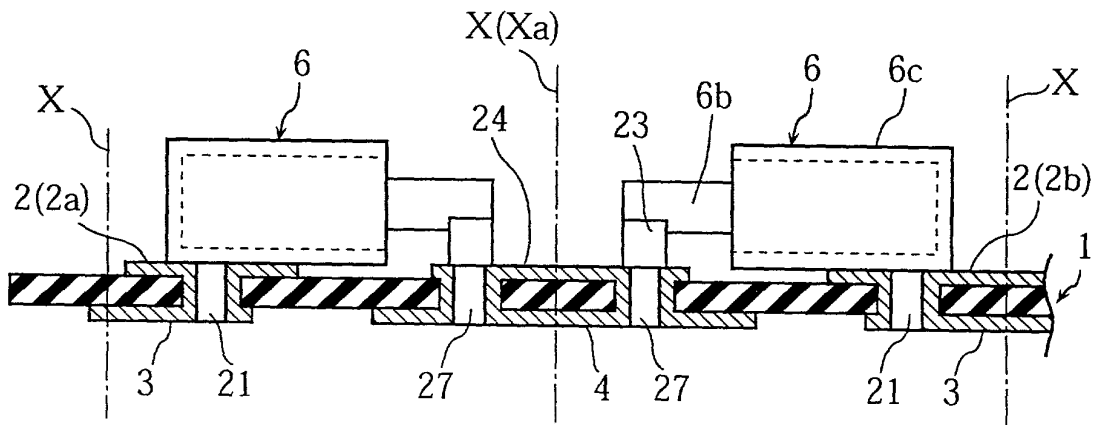


FIG. 133



62/73

FIG. 134

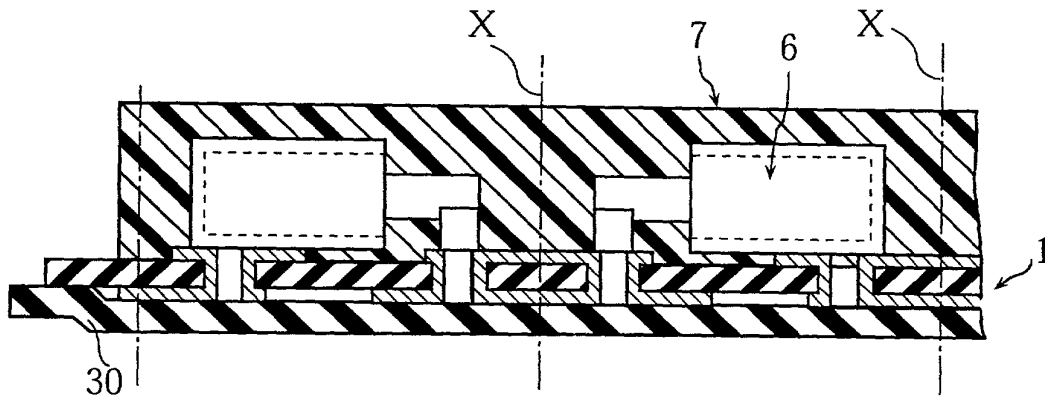
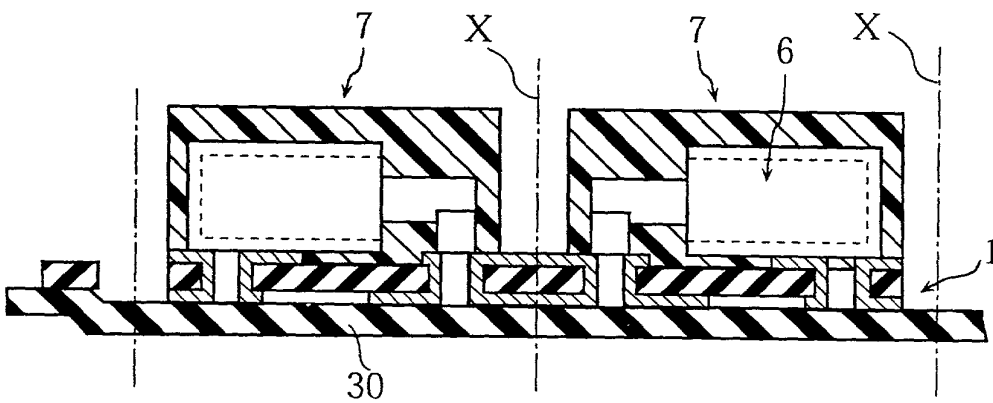


FIG. 135



*[The page contains faint, illegible markings or bleed-through from the reverse side.]*



*[The page contains faint, illegible markings or bleed-through from the reverse side.]*



64/73

FIG. 138

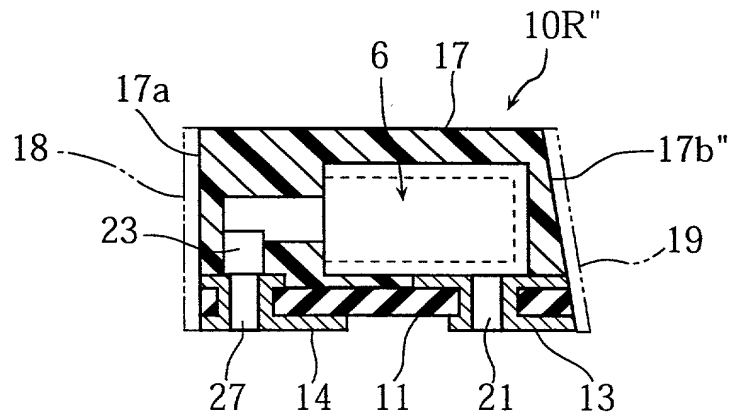
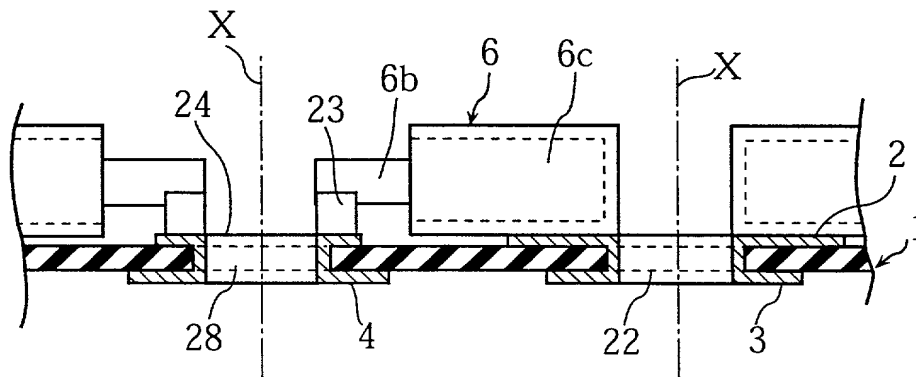


FIG. 139





65/73

FIG. 140

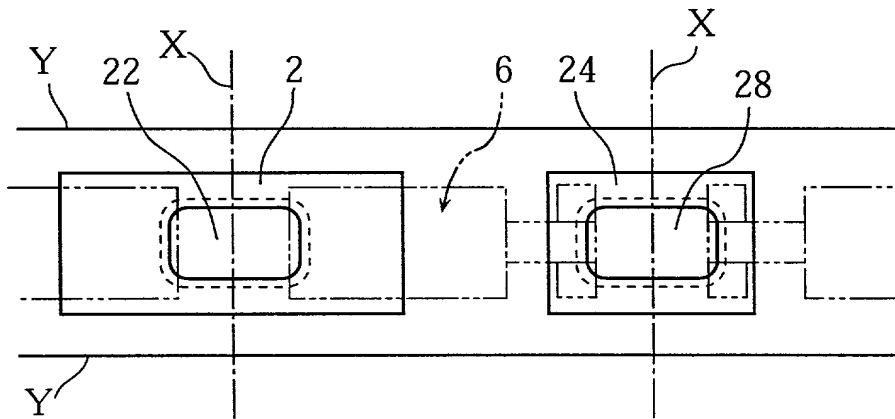
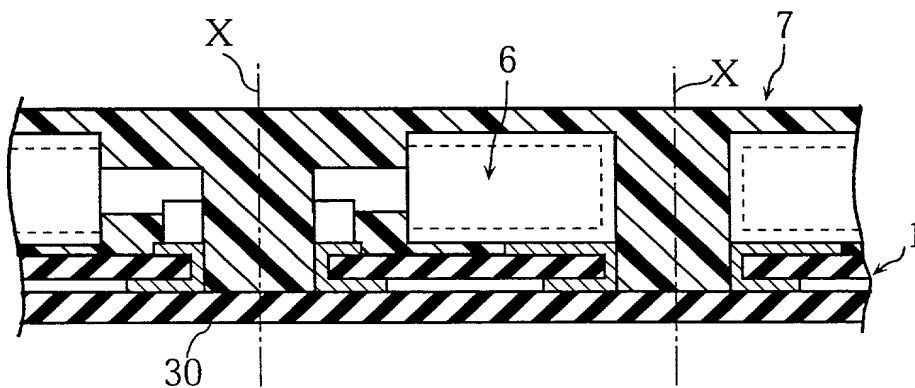


FIG. 141



66/73

FIG. 142

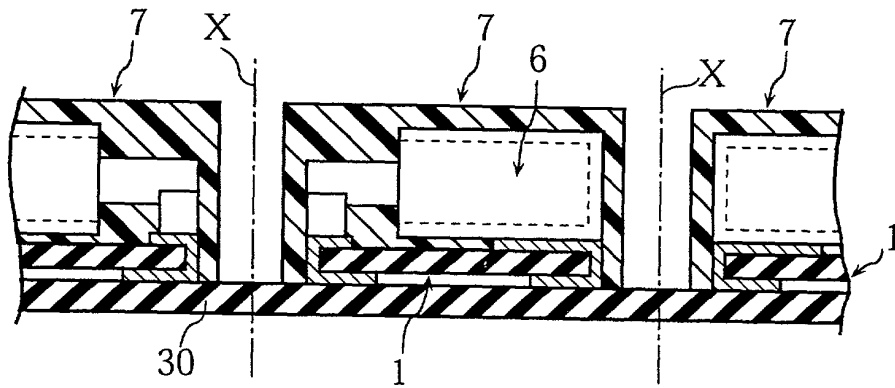
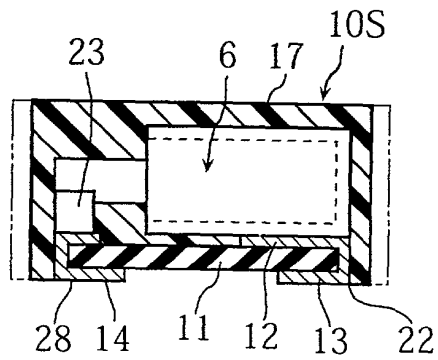


FIG. 143



67/73

FIG. 144

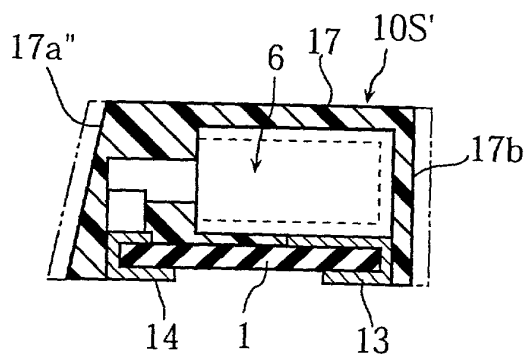
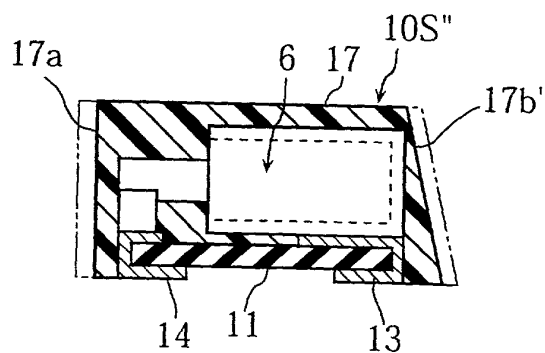


FIG. 145



68/73

FIG. 146

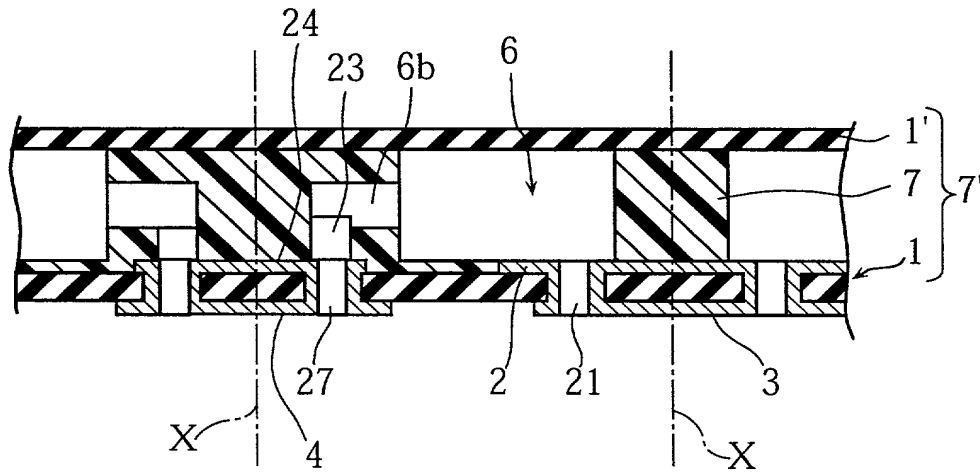
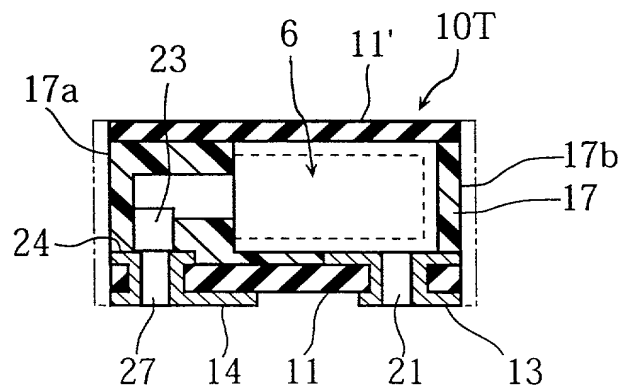


FIG. 147



69/73

FIG. 148

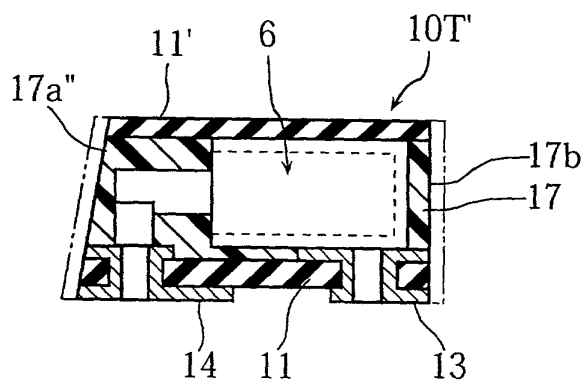
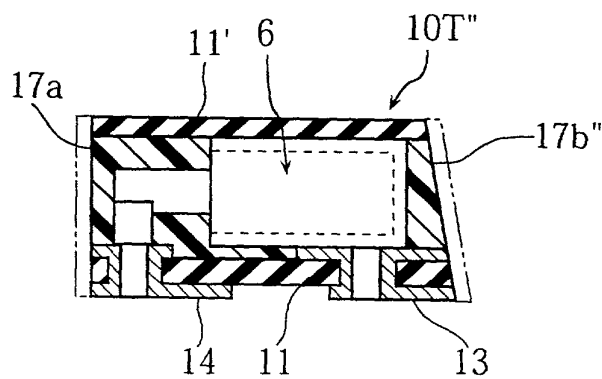


FIG. 149



70/73

FIG. 150

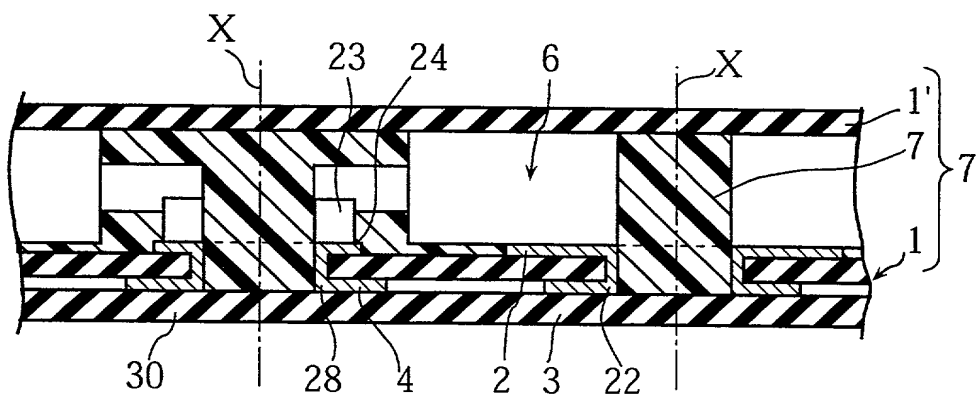
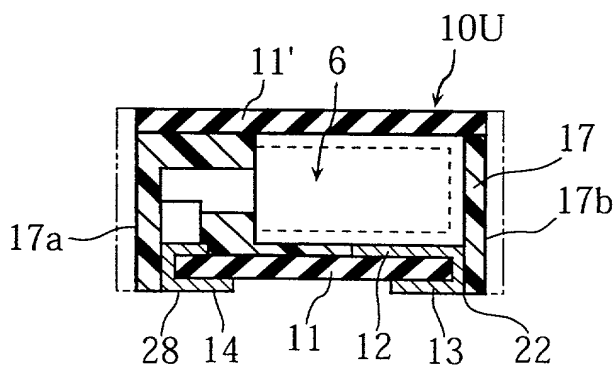


FIG. 151



71/73

FIG. 152

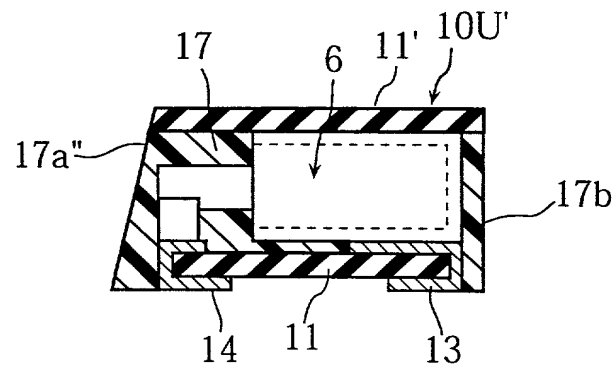
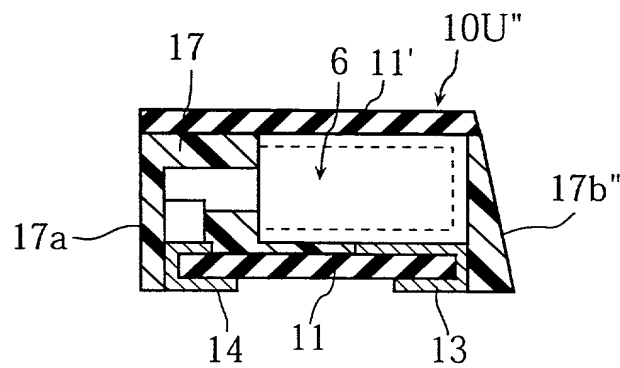


FIG. 153



72/73

FIG. 154  
PRIOR ART

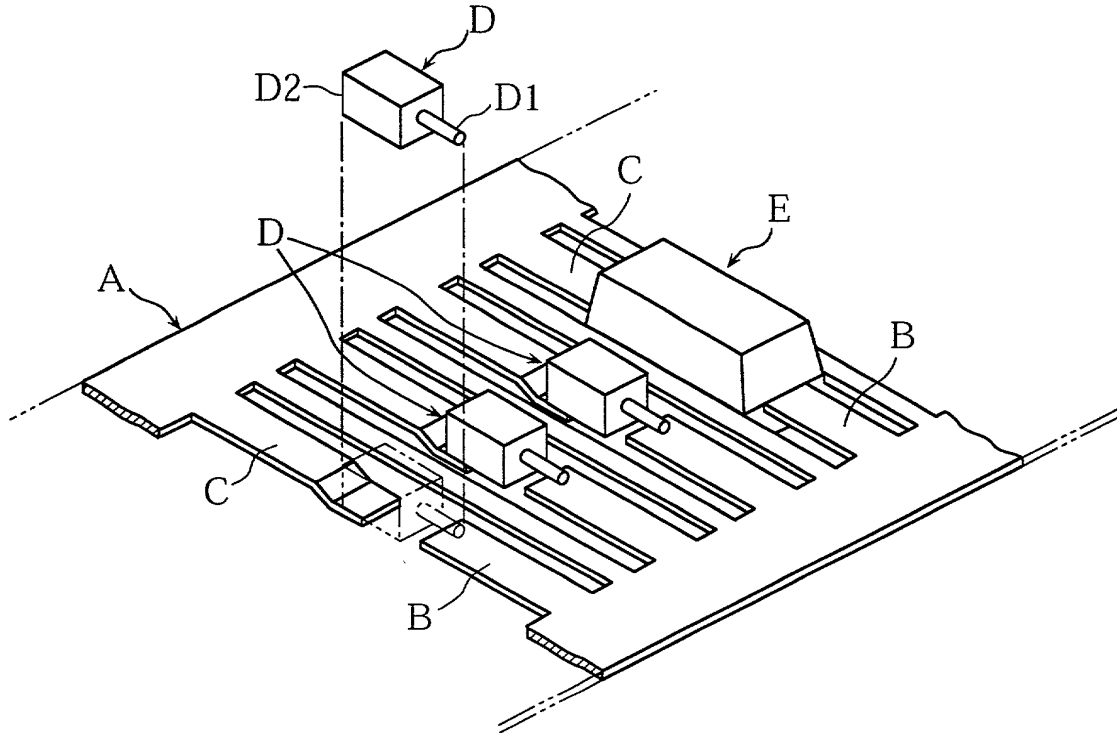
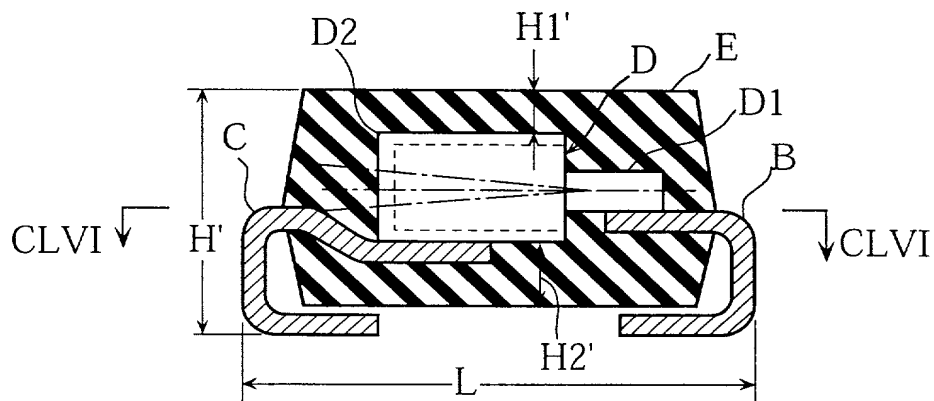


FIG. 155  
PRIOR ART





73/73

FIG. 156  
PRIOR ART

